HIGH-DEFINITION MULTIMEDIA INTERFACE

High-Definition Multimedia Interface

Compliance Test Specification

Version 1.0

Hitachi, Ltd.

Matsushita Electric Industrial Co., Ltd.

Philips Consumer Electronics, International B.V.

Silicon Image, Inc.

Sony Corporation

Thomson Inc.

Toshiba Corporation

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Preface

Notice

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Document Revision History

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1.0	2003/07/18	1.0 Release

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1 Introduction

1.1 Purpose and Scope

This document constitutes the specification of procedures, tools and criteria for testing the compliance of devices with the High-Definition Multimedia Interface Specification Version 1.0.

Each individual test is designed to ensure compliance with one or more requirements in the HDMI Specification or in one of its normative (required) specifications. No amount of testing can guarantee 100% interoperability among all passing devices when operated in all possible modes but, properly executed, the tests described in this document should give a very high level of confidence in the ability of the device to interoperate with other HDMI devices.

Due to the nature of testing a closed-box system such as a TV or DVD player, there are a variety of requirements in the HDMI Specification which are very difficult or impossible to directly verify. Compliance testing for these items will depend upon alternative methods which may not have 100% correlation with the HDMI-required behavior but will achieve the objective of generating confidence in the interoperability of the device.

Consumer Electronics Control (CEC) test methods are given in the HDMI Compliance Test Specification Supplement 1. Version 1.0 of Supplement 1 will be available shortly.

Type B and dual-link functionality is not fully covered by this test specification. Such details will be included in a future version.

1.2 Normative References

HDMI Licensing, LLC., “High-Definition Multimedia Interface, Specification Version 1.0”, December 9, 2002

Note that the HDMI Specification includes normative references affecting the required operation of HDMI devices.

1.3 Organization of this document

This specification is organized as follows:

- Chapter 1 describes the Purpose and Scope of the document, references, usages and conventions.
- Chapter 2 defines terms and acronyms used within the document.
- Chapter 3 provides an Overview to HDMI compliance testing.
- Chapter 4 describes the Required Capabilities for the defined test equipment as well as certain Recommended Test Equipment that has been proven to meet those requirements.
- Chapter 5 describes the tests for a Cable Assembly. For each test, a Required Test Method is described that defines the minimum requirements for accurate and valid testing and a Recommended Test Method that describes the specific procedure for the use of specific test equipment known to adequately test for the required condition.
- Chapter 6 describes the tests for Plug and Receptacles used on any HDMI product.
- Chapter 7 describes the tests for a Source.
- Chapter 8 describes the tests for a Sink

- Chapter 9 describes the tests for a Repeater.
- Appendix 1 lists the initial test equipment used by the Authorized Testing Centers.
- Appendix 2 describes the Software CRU technology used during TMDS electrical testing.
- Appendix 3 defines the Capabilities Declaration Form, which is filled out and submitted by the product manufacturer whenever a product is sent for testing at an Authorized Testing Center (ATC) or when the results of ATC or self-testing are sent to the HDMI Licensing, LLC.
- Appendix 4 defines the Test Results Form, which is completed by the test operator and submitted as the results of ATC or self-testing to the HDMI Licensing, LLC.
- Supplement 1: CEC, defines the tests for the optional Consumer Electronics Control protocol.

2 Definitions

2.1 Conformance Levels

expected	A key word used to describe the behavior of the hardware or software in the design models *assumed* by this specification. Other hardware and software design models may also be implemented.
may	A key word that indicates flexibility of choice with *no implied preferenc*e.
shall	A key word indicating a mandatory requirement. Designers are *required* to implement all such mandatory requirements.
should	A key word indicating flexibility of choice with a strongly preferred alternative. Equivalent to the phrase *is recommended*.

2.2 Usages and Conventions

Note that the HDMI Specification should be referenced for definitions of all usages and conventions that are not defined below.

bit N	Bits are numbered in little-endian format, i.e. the least-significant bit of a byte or word is referred to as bit 0.
D[X:Y]	Bit field representation covering bit X to bit Y (inclusive) of value or field D.
0xNN	Hexadecimal representation of base-16 numbers are represented using ‘C’ language notation, preceded by ‘0x’.
0bNN	Binary (base-2) numbers are represented using ‘C’ language notation, preceded by ‘0b’.
NN	Decimal (base-10) numbers are represented using no additional prefixes or suffixes.
!=	Does not equal (‘C’ notation).
==	Is Equal to (‘C’ notation). Used to test for a specific value (e.g. if bit 3 == 1, or, verify that byte SB0 == 0).
=	Equals (‘C’ notation). Used to assign a value to a variable (e.g. number of packets = number of pixels / 32) or is used in the specification of a required value (e.g. AVcc = 3.3V ±5%).
[HDMI: X.Y.Z]	Shorthand notation indicating a reference to the HDMI Specification. Examples: [HDMI: 3.2] denotes a reference to the HDMI Specification, section 3.2.
[CEC: X.Y.Z]	Denotes a reference to the HDMI Specification, Supplement 1, “Consumer Electronics Control”, section CEC X.Y.Z.

[861B: X.Y.Z]	Denotes a reference to the EIA/CEA-861B specification. Examples: [861B: 3.2] denotes a reference to the EIA/CEA-861B specification, section 3.2.
TMDS_DATA0	Equivalent to the differential signal pair TMDS Data0. When referring to a single-ended signal within this pair, TMDS_DAT0+ or TMDS_DATA0– is used. Same applies to TMDS_DATA1, TMDS_DATA2 and TMDS_CLOCK.
FAIL, “xxx”	Indicates a directive to the test operator to fail this test and to write “FAIL” in the “Pass/Fail” field of the Test Results form, and the comment “xxx” in the Comments field. It is permitted and frequently useful for the remainder of the test to be performed to provide additional information about the failure.
PASS, “xxx”	Indicates a directive to the test operator to pass this test and to write “PASS” in the “Pass/Fail” field of the Test Results form, and the comment “xxx” in the Comments field. The PASS directive indicates that the test is complete unless indicated otherwise. There is an implied PASS directive at the end of every test method, causing successfully completed tests to PASS.

2.3 Glossary of Terms

Note that the HDMI Specification should be referenced for definitions of any terms that are not defined below.

test coupon	A test trace, that emulates the signal traces, present on a test fixture PCB. The test coupon is used to measure and compensate for process variations during PCB manufacture.
support	The ability for a device to perform the appropriate action (for that device) with the specified format or option. For display devices, a video format is supported if such a signal is displayed in a manner comparable to other video formats or video from other inputs. For source devices, a video format is supported if the device is capable, after appropriate user input or delivery of appropriate content to the device, of outputting a signal with that format.
T_{BIT}	One bit time at the specified pixel clock frequency (= T_{PIXEL}/10). If no pixel clock frequency is specified, it is assumed to be the current (tested) pixel clock frequency.
T_{PIXEL}	One pixel time at the specified pixel (TMDS) clock frequency. If no pixel clock frequency is specified, it is assumed to be the current (tested) pixel clock frequency. If a video format is pixel-repeated, T_{PIXEL} continues to be defined as 10* T_{BIT}.

2.4 Acronyms and Abbreviations

Note that the HDMI Specification should be referenced for definitions of any terms that are not defined below.

ATC	Authorized Testing Center
CDF	Capabilities Declaration Form
DTD	Detailed Timing Descriptor (also called “18-byte timing descriptor)
DUT	Device Under Test
ISVM	I (current) Source Voltage Measurements
SVD	Short Video Descriptor (in Data Block collection of CEA EDID Timing Extension)
TDR	Time Domain Reflectometer/Reflectometry
TDT	Time Domain Transmission
TE	Test Equipment
TPA	Test Point Access
VSIM	Voltage Source I (current) measurements

3 Overview

HDMI system architecture is defined to consist of Sources, Sinks, Repeaters and Cable Assemblies. A given device may have one or more HDMI inputs and one or more HDMI outputs. Each HDMI input on a device shall follow all of the rules for an HDMI Sink and each HDMI output shall follow all of the rules for an HDMI Source. Consequently, each HDMI input shall be fully tested for compliance using the tests specified for Sink devices and each HDMI output shall be fully tested against the full set of tests specified for Source devices.

Any device with at least one HDMI input and at least one HDMI output is defined to be a Repeater. In addition to the Source and Sink tests required for each of the inputs and outputs, additional Repeater tests may be required.

In addition to the tests described for Sources, Sinks, Repeaters and Cable Assemblies, there are tests described for connectors present on these devices. The manufacturer of the device is required to verify the compliance of the connector in all cases, whether the product is ATC-tested or self-tested.

In order to provide the best coverage possible, it is necessary to perform many of the tests herein for each relevant operational mode of the Device Under Test (DUT). For instance, it is necessary to perform some of the video tests for each supported video format.

The primary purpose of the testing is to reveal whether the product passes all test cases. A failure of a single test item within a test case constitutes a failure of the product to meet the overall compliance testing requirement. However, even if an intermediate test step within a test case reveals a failure, it is permitted and frequently useful for the remainder of that test case and other test cases to be performed in order to provide additional information about the failure.

4 Test Equipment

4.1 Test Equipment Overview

4.1.1 Required Capabilities versus Recommended Equipment

Each piece of test equipment referenced by the individual test cases in the Source, Sink, Repeater and Cable Assembly sections is listed below. For each of these, the “Required Test Equipment Capabilities” are described. All equipment used for testing the related attributes shall comply with the requirements listed for that equipment.

In addition, for each of the defined pieces of equipment, specific commercial or custom “Recommended Test Equipment" is described. This is the equipment that is used in the initial HDMI Authorized Test Center and should also, if possible, be used for any self-testing of the related functions. Other configurations and equipment may be used for self-testing, as long as that equipment and the processes used meet all of the stated and implied requirements and permit an equivalent level of testing. It is the Adopter’s responsibility to verify that the substituted equipment and processes are sufficient.

4.1.2 Analyzers and Generators

In general, Source devices are tested using various Sink emulators with measurement functions, typically called “Analyzers”. These Sink emulators may have a variety of EDID structures used to encourage certain behavior by the Source DUT and they are capable of measuring a variety of parameters or attributes of the HDMI signals delivered by the Source DUT. The measurement may be performed using the facilities of the Sink emulator itself or using standard test equipment such as digital oscilloscopes, logic analyzers or network analyzers.

Likewise, Sink devices are tested using a variety of Source emulators or “Generators” capable of generating a variety of test signals. These generators may consist of custom hardware designed for HDMI compliance testing or may consist of standard waveform and pattern generators or some combination thereof.

4.1.3 Simultaneous Test Case Execution

Some test tools can be used for a variety of test cases. These tests can sometimes be executed simultaneously so that, with one running of the tool, several tests can be passed or failed without re-running the tool.

4.2 Test Equipment Requirements

All test equipment requiring calibration in order to ensure accurate and repeatable results shall be calibrated prior to and, if necessary, during the test procedure.

4.2.1 Electrical Testing

4.2.1.1 Test Point Access Boards

4.2.1.1.1 Overview

In order to gain access to the required signals, Test Point Access boards are required. TPA boards provide test points for all of the pins on the HDMI connector, including no-connect pins.

For each of the two different connector types (Type A and Type B) there are two different TPA board configurations. These are the Receptacle TPA (TPA-R) and Plug TPA (TPA-P) and are shown in Figure 4-1 and Figure 4-2. These boards permit direct access to all TMDS, DDC and CEC signals. Due to differences in the measurements taken (e.g. skew, jitter) and the types of probes used, there are a variety of TPA boards available of each type (Plug and Receptacle).

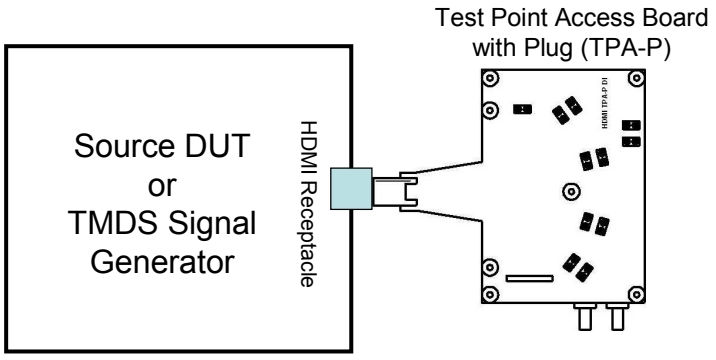


Figure 4-1 TPA-P, used for Source and Cable test calibration

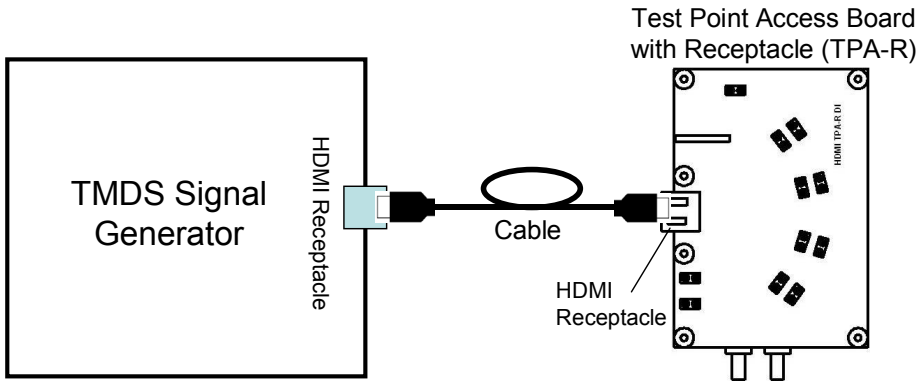


Figure 4-2 TPA-R, used for Sink and Sink test calibration

When a TPA board is acting as a Sink (for Source DUT testing), additional functionality is required. Termination resistors are connected between each TMDS signal and a (typically) 3.3V supply. In addition, a variety of EDID images may be required in order to get the Source to create the required signal. For this reason, an EDID Emulator may be attached to the TPA board. Lastly, as a Sink, the TPA is typically operated with the Hot Plug Detect signal connected to the +5V Power signal through a 1kohm resistor.

Required Test Equipment Capabilities

Following are the capabilities common among all of the TPA boards:

- HDMI plug or receptacle is mounted in such a way to enable direct connection to a Source, Sink or Cable Assembly.

- Termination: On any TPA that is used to emulate the behavior of a Sink, termination resistors are provided on each of the TMDS signal lines. In this case:
  - Connector is provided allowing input of external DC 3.3V source to +3.3V power rail used for TMDS termination.
  - Test point is provided on 3.3V rail.
  - Each single-ended TMDS signal is pulled up to +3.3V power rail through a 50 ohm resistor with less than ± 1% tolerance.
  - Test coupon test ports (see below) are pulled up to the +3.3V rail through a 50 ohm resistor with less than ± 1% tolerance. At least 1 GND pin is mounted near the test port (closer than 15mm).
- All TMDS signals have the following characteristics:
  - Test port shall be appropriate to the type of probe used and is located at an equivalent trace length from the HDMI connector as all other test ports.
  - Characteristic differential impedance of the connector, for each differential TMDS pair is 100 ohms ± 15%.
  - Characteristic differential impedance of the traces, for each differential TMDS pair, is 100 ohms ± 5% as a average over the entire trace. Peak impedance of up to 100 ohms ±10% is also permitted.
  - Intra-pair skew is less than 15psec.
  - Inter-pair skew is less than 40psec.
  - At least 1 GND pin is mounted near each TMDS test port. This pin is connected to the PCB ground plane as well as to all of the TMDS shields.
- Non-TMDS pins (if required for test):
  - These pins have testing ports that can be used to measure or drive each of the signals.
  - Connector is provided to allow input of DC 5V to the HDMI +5V Power pin.
  - HDMI HPD signal may be connected to HDMI +5V Power through a removable 1kohm resistor.
- Test coupon is recommended to be provided to measure and compensate for process variation of PCB manufacture:
  - Test coupon consists of one or two traces meant to emulate the traces of a single-ended TMDS signal or a differential pair of TMDS signals.
  - Each of the traces is located on the same layer of the PCB as the trace that it is emulating.
  - Trace length and characteristics are equivalent to that of the emulated trace on this board.
  - To enable easy and accurate attachment of testing equipment, each trace is terminated at one end to an SMA connector (or other connector of sufficient quality) and at the other with a Test port, which is identical to the Test ports for the TMDS signals and designed to match the probes used for the measurement.

4.2.1.1.2 TPA-P for Differential measurement

Access points are provided for differential probes to measure each of the four TMDS differential pairs.

Required Test Equipment Capabilities

- All standard TPA capabilities described above in Section 4.2.1.1.1.
- Type A plug connector is mounted to enable direct connection to a Source or Sink.
- TMDS test ports consist of two pins (for each TMDS differential pair) designed to allow direct and reliable connection of a differential probe.
- Test coupon consists of two traces as described in Section 4.2.1.1.1 with test ports identical to those on the TMDS traces.

Recommended Test Equipment

- Tektronix TPA-P-DI, available as one component in Tektronix 013-A013-50

4.2.1.1.3 TPA-R for Differential measurement

Access points for differential probes to measure across each of the four TMDS differential pairs.

Required Test Equipment Capabilities

- All standard TPA capabilities described above in Section 4.2.1.1.1.
- Type A receptacle connector is mounted to allow direct connection to a Cable Assembly.
- TMDS test ports consist of two pins (for each TMDS differential pair) designed to allow direct and reliable connection of a differential probe.
- Test coupon consists of two traces as described in Section 4.2.1.1.1 with test ports identical to those on the TMDS traces.

Recommended Test Equipment

- Tektronix TPA-R-DI, available as one component in Tektronix 013-A012-50

4.2.1.1.4 TPA-P for Single Ended measurement

Access points for single-ended probes to measure each of the TMDS single-ended signals.

Required Test Equipment Capabilities

- All standard TPA capabilities described above in Section 4.2.1.1.1.
- Type A plug connector is mounted to allow direct connection to a Source or Sink.
- TMDS test ports consist of two pins (for each TMDS single-ended signal) designed to allow direct and reliable connection of a single-ended probe with corresponding ground connection.
- Test coupon consists of one trace as described in Section 4.2.1.1.1 with test port identical to those on the TMDS traces.

Recommended Test Equipment

- Tektronix TPA-P-SE, available as one component in Tektronix 013-A013-50

4.2.1.1.5 TPA-R for Single Ended measurement

Access points for single-ended probes to measure each of the TMDS single-ended signals.

Required Test Equipment Capabilities

- All standard TPA capabilities described above in Section 4.2.1.1.1.
- Type A receptacle connector is mounted to allow direct connection to a Cable Assembly.
- TMDS test ports consist of two pins (for each TMDS single-ended signal) designed to allow direct and reliable connection of a single-ended probe with corresponding ground connection.
- Test coupon consists of one trace as described in Section 4.2.1.1.1 with test port identical to those on the TMDS traces.

Recommended Test Equipment

- Tektronix TPA-R-SE, available as one component in Tektronix 013-A012-50

4.2.1.1.6 TPA-P for TDR measurement

This TPA is typically used in a manner that emulates a Source device, rather than a Sink device.

Required Test Equipment Capabilities

- All standard TPA capabilities described above in Section 4.2.1.1.1.
- Type A plug connector is mounted to allow direct connection to a Source or Sink.
- TMDS test ports consist of one SMA connector for each TMDS signal and are designed to allow easy connection of a TDR oscilloscope.
- There are no TMDS pull-up resistors installed.
- Rise time of less than 200psec (10-90%), when connected to the TDR oscilloscope is possible.
- Test coupon consists of one trace as described in Section 4.2.1.1.1 with test port identical to those on the TMDS traces (SMA).

Recommended Test Equipment

- Tektronix TPA-P-TDR, available as one component in Tektronix 013-A013-50

4.2.1.1.7 TPA-R for TDR measurement

Required Test Equipment Capabilities

- All standard TPA capabilities described above in Section 4.2.1.1.1.

- Type A receptacle connector is mounted to allow direct connection to a Cable Assembly.
- TMDS test ports consist of one SMA connector for each TMDS signal and are designed to allow easy connection of a TDR oscilloscope.
- There are no TMDS pull-up resistors installed.
- Rise time of less than 200psec (10-90%), when connected to the TDR oscilloscope is possible.
- Test coupon consists of one trace as described in Section 4.2.1.1.1 with test port identical to those on the TMDS traces (SMA).

Recommended Test Equipment

- Tektronix TPA-R-TDR, available as one component in Tektronix 013-A012-50

4.2.1.1.8 TPA-R for Network Analyzer measurement (TPA-R-NA)

Required Test Equipment Capabilities

- All standard TPA capabilities described above in Section 4.2.1.1.1.
- Type A receptacle connector is mounted to allow direct connection to a Cable Assembly.
- TMDS test ports consist of one SMA connector for each TMDS signal and are designed to allow easy connection of a Network Analyzer.
- Measurement bandwidth is 300kHz - 4.125GHz
- Rise time of less than 200psec, when connected to the TDR oscilloscope is possible.
- Test coupon is preferred but not required.

Recommended Test Equipment

- ADVANTEST CAX-ATI013

4.2.1.2 Jitter/Eye Analyzer

All jitter and eye measurements are taken relative to a Recovered Clock which is generated by a Clock Recovery Unit (CRU). This recovered clock is meant to approximate the Ideal Recovery Clock specified in the HDMI Specification. This Recovered Clock, rather than the real TMDS differential clock, is used as the trigger for measurement of the TMDS clock jitter and TMDS data eye diagram.

Figure 4-3 shows *functionally* how the CRU is used to measure an eye diagram. Clock jitter is measured using a very similar approach, shown in Figure 4-4. Effectively, the CRU generates the trigger which the oscilloscope uses to capture and display the data eye.

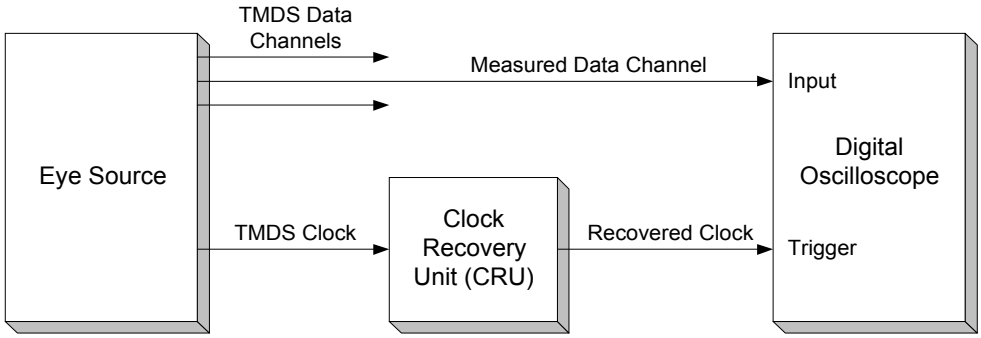


Figure 4-3 TMDS Eye Diagram Measurement: 10x clock output from CRU(bit time)

Figure 4-4 shows how the CRU is used to measure the jitter on a transmitted TMDS clock.

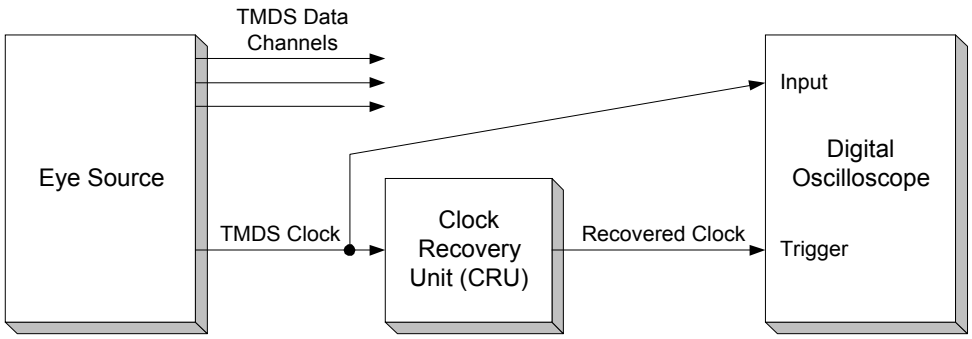


Figure 4-4 TMDS Clock Jitter Measurement: 1x clock output from CRU (pixel time)

In actuality, the recommended CRU consists of software which digitally processes captured data. Following the capture, the software CRU processes the captured TMDS_CLOCK waveform according to the mathematical definition of the Ideal Recovery Clock, specified in [HDMI: 4.2.3]. The eye diagram is then drawn as if a series of captures had occurred, each triggered by a Recovered Clock edge.

This type of approach can be made to work with any analog data capture device with sufficient resolution, speed, memory depth and jitter-free capture clock. Following the capture, the software CRU algorithm could process and display data on any computer. A digital oscilloscope may be used to provide the data capture, software processing and/or display capabilities required.

This software approach is recommended, due to the high correlation between the software implementation and the mathematical definition of the Ideal Recovery Clock.

Jitter and eye measurements are used for Source, Sink, and Cable Assembly compliance testing. For Source testing, the Jitter/Eye Analyzer is used to verify the compliance of the output eye and TMDS clock jitter directly. For Sinks, the Jitter/Eye Analyzer is used during the calibration of a worst-case eye from a TMDS Signal Generator. The worst-case eye is input to the Sink to determine its data recovery capabilities. For cables, generation of a worst-case input eye as well as analysis of the cable's output eye are performed.

Required Test Equipment Capabilities

The Jitter/Eye Analyzer must be capable of accurately indicating the amount of jitter or the actual eye diagram on the tested TMDS differential signal.

The transfer function for an Ideal Recovery Clock is shown in Equation 4-1 below. An ideal CRU would perfectly match this function.

Across the tested clock frequency range, the Jitter/Eye Analyzer's CRU shall have a jitter transfer amplitude that differs, from the ideal transfer function, by no more than ±0.2dB from DC to 10MHz. At 20MHz the difference must be less than ±1dB and at 50MHz, less than +2/-6dB. From DC to 20MHz, the jitter transfer phase response must be within ±1.8 degrees of the phase response of the ideal recovery clock.

$$H(j\omega) = 1 / (1 + j\omega/\omega_0)$$

Where $\omega_0 = 2\pi F_0$, $F_0 = 4.0MHz$

Equation 4-1 Jitter Transfer Function of PLL for Ideal Recovery Clock Definition

Recommended Test Equipment

The Recommended Jitter/Eye Analyzer uses a high-speed digital oscilloscope to perform the data capture operation and a PC to perform the software CRU processing and display:

- Tektronix TDS7404 4GHz Digital Oscilloscope, with 32 mega-samples total (16 mega-samples on each of two active channels).
- Two (2) Tektronix P7330 Differential Probes
- PC running 32-bit Windows OS (may be integrated into oscilloscope)
- Tektronix SoftCRU software, running on the Windows PC, designed to be used with the data captured from the Tektronix TDS7404 digital oscilloscope. (See Appendix 2 for details.)

4.2.1.3 4GHz Digital Oscilloscope

Required Test Equipment Capabilities

- DC to 4GHz, -3dB bandwidth or greater
- Input configurations:
  - 1 or 2 Differential Probes
  - 1 or 2 Single-Ended probes
- Sampling rate >= 10GSample/sec, sampling 2 channels simultaneously.
- Sample memory: >=32 mega-samples total (>=16 mega-samples on each of two active channels).

Recommended Test Equipment

- Tektronix TDS7404 4GHz Digital Oscilloscope with large memory option (#4M)

4.2.1.4 Differential Probe

Required Test Equipment Capabilities

- DC - 3.5GHz bandwidth (or greater) when connected to the oscilloscope
- Can connect directly and reliably to the TPA-P-DI or TPA-R-DIfixtures
- Length of Ground Lead is less than 7cm

Recommended Test Equipment

- Tektronix P7330 Differential Probe
  - Tektronix 016-1884-00 Square Pin Adapter
  - Tektronix 196-3469-00 Ground Lead

4.2.1.5 Single-Ended Probe

Required Test Equipment Capabilities

- DC - 4GHz bandwidth (or greater) when connected to the oscilloscope .
- Can connect directly and reliably to the TPA-P-SE or TPA-R-SE fixtures

Recommended Test Equipment

- Tektronix P7240
  - Tektronix 016-1773-00 Square pin socket

4.2.1.6 SMA Cables

Required Test Equipment Capabilities

- Less than 2 meters, preferably less than 1 meter.
- Bandwidth: 9GHz or greater
- 50 ohms impedance

Recommended Test Equipment

Any of the following are sufficient:

- Tektronix 174-1428-00 (1.5 meter)
- Tektronix 174-1341-00 (1 meter)

4.2.1.7 50 Ohm SMA Terminators

Required Test Equipment Capabilities

- 50 ohms impedance ± 1% or better
- Connects directly to SMA female.

Recommended Test Equipment

Any lab-quality terminator which meets requirements above is sufficient.

4.2.1.8 TMDS Signal Generator

Generates HDMI signal with a variety of patterns, clock jitter, data waveform (eye diagram) and amplitude characteristics.

Required Test Equipment Capabilities

Capable of outputting an HDMI signal with the following characteristics:

- Video format:
  - 720x480p @ 59.94Hz
  - 1920x1080i @ 60Hz
  - 1280x720p @ 60Hz
  - 720x576p @ 50Hz
  - 1920x1080i @ 50Hz
  - 1280x720p @ 50Hz
- Video Data
  - RGB pixel encoding: Repeating gray scale ramp 0, 1, 2…254, 255, 0, 1, 2…during each active video period
  - YC_BC_R 4:4:4 pixel encoding: Repeating gray scale ramp. This should display the same as the RGB gray ramp, i.e. the displayed ramp should increment every pixel.
- Audio format:
  - 16-bit L-PCM 48kHz sampling frequency, N and CTS values (constant) per [HDMI: Table 7-3].
- Audio data:
  - 1KHz sine wave with amplitude of –18 dBFS (full scale) on Left channel
  - 400Hz sine wave with amplitude of –18 dBFS (full scale) on Right channel
- +5V Power always set to +5.0V
- TMDS Clock with the ability to add the following sinusoidal Jitter components
  - 1MHz and 7MHz. NOTE: the 1MHz component is used to emulate data jitter, while the 7MHz component is used to emulate clock jitter.
  - 500kHz and 10MHz. NOTE: the 500kHz component is used to emulate data jitter, while the 10MHz component is used to emulate clock jitter.

- The amplitude of all jitter components can be adjusted independently from 0.0 to 7.4nsec with resolution of 10psec

- Data Eye shape
  - Rise time, fall time 140psec (typical)
  - Overshoot ≤10% of differential 1Vp-p swing.
  - Undershoot ≤10% of differential 1Vp-p swing.
- Output voltage levels (when driving a 50 ohm termination to 3.3V):
  - 2.5V to 3.3V
  - Independent amplitude control for each of 4 TMDS channels
- Differential swing range (data channels only):
  - 0V (±0.06V) to 2.5Vp-p in 10mV steps
- Channel-to-channel skew range:
  - 37 nsec (i.e. 1 T_{PIXEL} @ 27MHz pixel clock)

Recommended Test Equipment

The recommended TMDS Signal Generator consists of the following major components:

- (1) Tektronix DTG5274 2.7GHz Digital Timing Generator (DTG)
  - (3) Tektronix DTGM30 output modules for DTG5274
  - (2) Tektronix 012-1503-00 Pin Header SMB 51cm (20in.)
  - (2) Tektronix 015-0671-00 SMB-BNC adapter
- (1) Tektronix AWG710 Arbitrary Waveform Generator
- (2) Mini-circuits ZFBT-4R2GW Bias-Tee
  - (2) BNC-SMA adapters (1 for each Bias-Tee)
- (12) SMA Cables: either Tektronix 174-1428-00 (1.5 meter) or Tektronix 174-1341-00 (1 meter), as needed to connect output of equipment to TPA boards and to deliver synchronization signal(s) from AWG to DTG

4.2.1.9 Network Analyzer

Required Test Equipment Capabilities

- 4 ports used simultaneously
- At least 300kHz - 4.125GHz bandwidth is available.
- Dynamic accuracy is ≤ (±)0.50dB from 0 to – 50dBm, over the frequency range 300kHz - 4.125GHz.

Recommended Test Equipment

- ADVANTEST R3860
- ADVANTEST R17051 (Auto Cal KIT)

4.2.1.10 TDR/TDT Oscilloscope

Required Test Equipment Capabilities

- TDR measurement
  - Bandwidth : ≥ 20GHz
  - Pulse rise time : ≤ 35ps (10-90%)
  - 2 port (1 differential in-out)
  - Ability to adjust the rise time of the TDR waveform that is displayed on the screen to ≤ 200 ps (10-90%)
- TDT measurement
  - Bandwidth: ≥ 20GHz
  - Pulse rise time : ≤ 35ps (10-90%)
  - 4 port (1 differential out and 1 differential in)

Recommended Test Equipment

- Tektronix TDS8000B
- Tektronix 80E04 TDR-module
- Tektronix 80E03 Sampling module

4.2.1.11 Digital Multi-Meter and Probe

Required Test Equipment Capabilities

- Basic DC voltage, DC current, DC resistance measurement capability as well as ISVM and VSIM capabilities.
- Both ISVM function and VSIM function capability
  - ISVM: Can measure the voltage with controlling the max drain current
  - VSIM: Can measure the current with controlling the output voltage.
- Indicate the value of the DC resistance as a digital number.
- DC resistance resolution is more than 3 digits.
- DC resistance accuracy is ≤ ±1%.
  - In-circuit test capability: range 0 - 100 ohms must be measured.
  - At least 1Mega-ohm (disconnected) must be measured.
- Indicates the value of the DC voltage as a digital number.
- DC voltage resolution is smaller than 10mV when range is more than 10V.
- DC voltage accuracy is ≤ ±1%

Recommended Test Equipment

- ADVANTEST R6240A

4.2.1.12 Voltage Meter

Required Test Equipment Capabilities

- DC voltage resolution ≤ 1µV when range is 0-1mV.
- DC voltage accuracy ≤ ±10µV when range is 0-1mV.

Recommended Test Equipment

- ADVANTEST R6552

4.2.1.13 Resistor for HPD Test

Required Test Equipment Capabilities

- For Sink testing; 10Kohms ≤ ±1%, 0.25W
- For Source testing 1.2Kohms ≤ ±1%

Recommended Test Equipment

Any resistor with the Required Capabilities is sufficient.

4.2.1.14 DC power supply

Required Test Equipment Capabilities

- Can output DC 3.3V and 5V with accuracy of ≤ ±1%
- Maximum output current can be set with accuracy of ≤ ±5% over the 10 to 100mA range.

Recommended Test Equipment

- KENWOOD PW18-1.8AQ

4.2.1.15 LCR Meter

Required Test Equipment Capabilities

- Test signal specification
  - Frequencies: 100kHz and 1kHz
  - AC level : 2.5Vp-p
  - DC level : 2.5V
- Resolution is equal or less than 1pF
- Accuracy is equal or less than 1pF

Recommended Test Equipment

- HIOKI 3522-50 Digital LCR Meter
- HIOKI 9143 Probe

- HIOKI 9268 DC Bias unit

4.2.1.16 HDMI Cable Emulator

Required Test Equipment Capabilities

A different cable may be required for each different tested pixel clock frequency.

- Type A Plug connectors are mounted on both ends of the cable.
- TMDS_DATA jitter degradation of 0.2 T_{BIT} ± 0.015 T_{BIT} measured at the crossing point. Jitter inherent in the input signal must be measured and subtracted from the output jitter for this measurement. This degradation is measured when the cable is driven with a TMDS signal that includes 0.3 T_{BIT} of 1MHz data jitter and 0.25 T_{BIT} of 7MHz clock jitter (as measured with CRU).
- TMDS_CLOCK jitter degradation of between 0.05 T_{BIT} ± 0.03 T_{BIT} measured at the zero volt level. Jitter inherent in the input signal must be measured and subtracted from the output jitter for this measurement. This degradation is measured when the cable is driven with a TMDS signal that includes 0.3 T_{BIT} of 1MHz data jitter and 0.25 T_{BIT} of 7MHz clock jitter (as measured with CRU).

Recommended Test Equipment

- For 74.25MHz tests: JAE DC1P19ST07425AA
- For 27MHz tests: JAE DC1P19ST02700AA

4.2.2 Connector Testing

There are a number of tests designed to verify compliance of the connector with HDMI-specified dimensions or performance. The HDMI Compliance Test Specification does not attempt to describe the test equipment or processes required for this testing.

4.2.3 EDID Testing

4.2.3.1 EDID Reader/Analyzer

The Sink's EDID is read and evaluated by the EDID Reader/Analyzer.

Required Test Equipment Capabilities

The EDID Reader/Analyzer shall be capable of:

- reading all bytes of all blocks within the EDID,
- presenting the entire contents of the EDID to the operator in an easily understandable format
- detecting and clearly indicating to the operator the failure to comply with at least some of requirements referenced in Section 8.2.
- allowing the operator to manually but easily identify compliance with the remaining items in Section 8.2.

Recommended Test Equipment

The recommended EDID Reader/Analyzer consists of the following components:

- Silicon Image TE9100 EDID Tester Kit.
- PC running Windows 32-bit OS.

The Silicon Image TE9100 consists of the following:

- Silicon Image EDID Tester PCB. This hardware provides a variety of EDID-related functions. In this use, it can be attached to a Sink DUT in order to read the entire contents of the EDID within the Sink.
- Serial cable. Connected between the PC and the EDID Tester PCB, allowing the PC to acquire the EDID image read from the Sink.
- Silicon Image EDID Analyzer / Editor Software operating in “HDMI Compliance” mode. This software is designed to parse the contents of the Sink DUT EDID per the HDMI Specification, VESA E-EDID 1.3, and EIA/CEA-861B.

To use this equipment as an EDID Reader/Analyzer do the following:

- Connect the PC to the EDID Tester PCB using the serial cable.
- Connect the EDID Tester PCB to the HDMI input connector under test.
- Run the EDID Analyzer/Editor software.

4.2.3.2 EDID Emulator

An EDID image may be presented to a Source DUT by connecting an EDID Emulator to the SDA and SCL signals on any of the standard TPA fixtures.

Required Test Equipment Capabilities

The EDID Emulator shall be capable of:

- presenting a 4-block (512-byte) EDID to a Source
- connecting to the +5V Power, SDA and SCL signals of any standard TPA fixture.
- adding sufficient capacitance to SDA and SCL signals in order to reach maximum allowed capacitance (750pF).

Recommended Test Equipment

The recommended EDID Emulator includes:

- Silicon Image TE9100 EDID Tester Kit.
- PC running Windows 32-bit OS.

The Silicon Image TE9100 consists of the following:

- Silicon Image EDID Tester PCB. This hardware provides a variety of EDID-related functions. In this use, it can be attached to a Source DUT in order to provide a complete Sink emulation function at the TPA.

- Serial cable. Connected between the PC and the EDID Tester PCB, allowing the PC to acquire the EDID image read from the Sink.
- Silicon Image EDID Analyzer / Editor Software. This software is designed to enable the operator to create and edit EDID images per the HDMI Specification, VESA E-EDID 1.3, and EIA/CEA-861B and to download those images into the EDID Tester PCB.

To use this equipment as an EDID Emulator do the following:

- Connect the PC to the EDID Tester PCB using the serial cable.
- Connect the EDID Tester PCB to the TPA fixture's SDA, SCL, +5V Power and Ground signals.
- Run the EDID Analyzer/Editor software and download the appropriate image.
- Press the HPD button for ½ second or so to notify the Source DUT of the new EDID image.

4.2.3.3 I^2C Analyzer

An I^2C analyzer is required to test E-DDC.

Required Test Equipment Capabilities

The I^2C analyzer shall be capable of:

- Displaying all elements of an I^2C transaction in a manner that allows the operator to determine if the transaction is compliant with the E-DDC protocol.
- Ability to be connected to the SDA and SCL signals on an EDID Emulator PCB or TPA fixture.

Recommended Test Equipment

- Yokogawa DL1640/F5 Oscilloscope (includes I^2C Analyzer option)

4.2.4 Protocol Testing

4.2.4.1 Encoding Analyzer

The Encoding Analyzer is used to verify correct low-level encoding by the Source DUT.

Required Test Equipment Capabilities

The Encoding Analyzer is capable of analyzing an HDMI signal and detecting the following:

- Any illegal 10-bit code generated by a Source on any of the three channels. Legal codes are limited to the following:
  - Any legal Video Data codes
  - 4 Control Period codes
  - 16 TERC4 codes
  - 4 Data Island Guard Band codes

- Video Guard Band code

- Any Video Data Code that was encoded with an incorrect “data stream disparity” value, that is, which causes the channel to become more, rather than less DC-balanced.
- Any pixel that does not use a consistent coding method across all three TMDS channels.

The Encoding Analyzer should be capable of recovering the data from any compliant HDMI signal with a bit error rate of better than 10^{-9}. The Encoding Analyzer shall be designed assuming no data recovery errors. On occasion, a test may therefore fail due to a rare, but permitted, data recovery error. The operator may re-run the test in the case of these intermittent errors.

The Encoding Analyzer shall be capable of attaining character synchronization (detection of the start of the 10-bit code on each channel) following the reception of 12 contiguous Control Period-encoded pixels and of maintaining the synchronization for the duration of the data capture.

Recommended Test Equipment

The P/A/V Analyzer is recommended for use as an Encoding Analyzer.

- Protocol/Audio/Video Analyzer described below

Protocol/Audio/Video Analyzer

The Recommended Test Method for most of the Source Protocol tests as well as some of the Source Audio (7.6) and Video (7.5) tests, is based on the P/A/V Analyzer. This tool can act as an recommended Encoding Analyzer, Protocol Analyzer, Audio Timing Analyzer and Video Timing Analyzer.

This tool consists of the following components:

- TMDS Capture Board
- Personal Computer running a Windows 32-bit OS with an IEEE1394 port available and connected to the TMDS Capture Board for downloading the captured TMDS sequences.
- HDMI Analysis Software running on the PC
- IEEE1394 cable connected between TMDS Capture Board and PC

The HDMI Analysis software has the following major features:

- Can download the data file from the TMDS Capture Hardware
- Can execute several commands selected via menus that perform different groups of tests.
- Can output the results of the tests on-screen and/or to a text file, indicating, for each test performed, a PASS or FAIL result.
- Can output a processed HDMI protocol sequence data file, outlining the positions of Data Islands, specific packet types, Video Data Periods, Preambles, etc. and including markers indicating at the positions in the sequence where specific tests failed.

The Recommended Test Methods using the P/A/V Analyzer will describe which HDMI Analysis commands are executed and what the indication will be if that test fails or passes.. Following are the configuration and operation instructions for the P/A/V Analyzer.

- Connect Source DUT to the TMDS Capture board with an HDMI cable.

- Connect the TMDS capture board to the PC with a IEEE1394 cable.
- If required, connect a Timer/Counter to the appropriate test points and set to Frequency mode.
- Operate the Source DUT as described in the Recommended Test Method.
- Initiate the “Capture” operation of the TMDS Capture board. Continue the operation of the Source DUT for the duration of the capture.
- Run the HDMI Analysis software on the PC.
- Select the HDMI Analysis “Download Capture” command. If needed, input the pixel clock frequency value read from the Timer/Counter. Save the capture file.
- Select the command specified in the Recommended Test Method and select the capture file just saved.
- Examine the output of the HDMI Analysis software for the indication described in the Recommended Test Method and document the results in the Test Results Form as instructed.

4.2.4.2 Protocol Analyzer

The Protocol Analyzer is used to detect protocol errors generated by a Source. Proper operation of the Protocol Analyzer is only guaranteed if the Source DUT passes all tests in Section 7.2, 7.3 and Test ID 7-16: Legal Codes.

Required Test Equipment Capabilities

The Protocol Analyzer data recovery and character synchronization performance requirements are identical to those of the Encoding Analyzer.

On occasion, a test may therefore fail due to a rare, but permitted, data recovery error. The operator may re-run the test in the case of these intermittent errors.

The Protocol Analyzer shall be capable of determining whether each Protocol element is compliant with the requirements described in the Source Protocol tests section. These include, but are not limited to:

- Preamble values.
- Relative placement or length of Preambles, Guard Bands, Data Islands, Control Periods, etc.
- BCH parity bits for any of the five ECC blocks in every packet.

Recommended Test Equipment

The P/A/V Analyzer is recommended for use as a Protocol Analyzer.

4.2.4.3 TMDS Protocol Generator

Required Test Equipment Capabilities

The Protocol Generator shall be capable of transmitting the following:

- A compliant HDMI signal consisting of an RGB video test pattern at either 720x480p @ 59.94Hz or 720x576p @ 50Hz, with 2-channel 48kHz PCM audio.
- All variations of this basic signal described in Section 8.4, Sink – Protocol.

Recommended Test Equipment

The Recommended TMDS Signal Generator consists of the following major components:

- Tektronix DTG5274 Digital Pattern/Timing Generator
- Tektronix DTM30 (3pcs) output module for DTG5274
- TPA-P-TDR (in some test configurations, where driving a Sink directly)
- SMA Cables as needed to connect output of equipment to TPA boards

4.2.5 Audio/Video Testing

4.2.5.1 Video Timing Analyzer

The Video Timing Analyzer analyzes the relative timing of pixels, HSYNC, VSYNC and Video Data Periods, and absolute pixel clock frequency, and uses this information to determine compliance with the relevant specifications. Proper operation of the Video Timing Analyzer is only guaranteed if the Source DUT passes all tests in the Source Protocol section.

Required Test Equipment Capabilities

The Video Timing Analyzer examines the transmitted video timing and shall be capable of:

- determining the exact number of TMDS pixel clocks within the horizontal front porch, HSYNC pulse, back porch and Video Data Period (excluding the Video Guard Band).
- determining the HSYNC polarity (positive or negative),
- determining the exact number of video lines within the vertical front porch, VSYNC pulse, back porch and active data period,
- determining the VSYNC polarity (positive or negative),
- determining the exact offset (in TMDS pixel clocks) of the active edge of VSYNC from to the active edge of HSYNC,
- determining the TMDS pixel clock frequency with an accuracy of ±0.01%
- determining, or allowing the operator to determine, if all of the above values match the required values specified in EIA/CEA-861B.

Recommended Test Equipment

The P/A/V Analyzer is recommended for use as an Video Timing Analyzer.

4.2.5.2 Video Picture Analyzer

Required Test Equipment Capabilities

The Video Picture Analyzer allows the operator to view or otherwise examine the contents of the transmitted video and shall be capable of:

- presenting to the Source DUT, a specific EDID image selected by the operator,
- accurately indicating the contents of any and all AVI InfoFrames transmitted by the Source DUT,
- Shall be capable, through operator observation, of accurately indicating the aspect ratio of the transmitted picture, assuming that the picture content provides sufficient clues (circles or other obvious structures).

Recommended Test Equipment #1

The first recommended Video Picture Analyzer consists of the following components:

- Protocol/Audio/Video Analyzer, described above based on TMDS Capture Board

Recommended Test Equipment #2

A second recommended Video Picture Analyzer consists of the following components:

- Silicon Image TE9001 kit, acting as an HDMI→Component Analog Video converter and AVI InfoFrame capture tool
- Any television or monitor which accepts component analog video input with all of the following timings and is capable of displaying the received video with sufficient color accuracy to enable an operator to determine if the transmitted video is in YC_BC_R or RGB color space.
  - 480i @ 59.94/60Hz
  - 480p @ 59.94/60Hz
  - 1080i @ 59.94.60Hz
  - 720p @ 59.94.60Hz
  - 576i @ 50Hz
  - 576p @ 50Hz
  - 1080i @ 50Hz
  - 720p @ 50Hz
- Silicon Image software “HDMI Gear”, running on a Windows PC, indicating to the user the contents of the captured AVI InfoFrames

4.2.5.3 Audio Timing Analyzer

The Audio Timing Analyzer analyzes the timing and content of audio-related packets and of using this information to determine compliance with the relevant specifications. Proper operation of the Audio Timing Analyzer is only guaranteed if the Source DUT passes all tests in the Source Protocol section.

Required Test Equipment Capabilities

The Audio Timing Analyzer shall be capable of the following:

- Extracting the ACR, Audio Sample Packets and accurately timing the number of pixel clocks since the arrival of the previous such packet.
- Extracting the Audio InfoFrame Packets and timing their arrival to determine which video field the packet was transmitted in.
- Extracting the audio sample size, sample rate, and sample rate accuracy encoded within the Channel/Status bits of the Audio Sample Packets.
- Extracting the N and CTS values from the ACR Packets.
- Determining the TMDS pixel clock frequency with an accuracy of ±1ppm.
- Using the above information to determine whether these values and timings are within the requirements of the HDMI 1.0 and IEC 60958 specifications.

Recommended Test Equipment

The P/A/V Analyzer is recommended for use as an Audio Timing Analyzer.

4.2.5.4 Audio/Video Protocol Generator

Sink DUTs capable of receiving audio are tested using an Audio/Video Protocol Generator.

Required Test Equipment Capabilities

- The Audio/Video Protocol Generator shall be capable of operating in two modes:
  - outputting a DVI signal carrying:
    - a valid video signal using RGB pixel encoding, or,
  - outputting an HDMI signal carrying:
    - a valid video signal using RGB pixel encoding and,
    - a valid IEC60958 audio signal
    - a valid Audio InfoFrame
- …where the video signal may be configured to be any one of the following EIA/CEA-861B Video Format Timings that is supported by the Sink DUT:
  - 640x480p @ 59.94Hz -0.5% and @ 60Hz+0.5%
  - 720x480p @ 59.94Hz -0.5% and @ 60Hz+0.5%
  - 1280x720p @ 59.94Hz -0.5% and @ 60Hz+0.5%
  - 1920x1080i @ 59.94Hz -0.5% and @ 60Hz+0.5%
  - 720x576p @ 50Hz-0.5% and @ 50Hz+0.5%
  - 1280x720p @ 50Hz-0.5% and @ 50Hz+0.5%
  - 1920x1080i @ 50Hz-0.5% and @ 50Hz+0.5%
- …and where the audio signal consists of a 1kHz sine wave or other readily identifiable test signal and may be configured to use any of the following formats supported by the Sink DUT:
  - PCM at 32, 44.1, 48, 88.2, 96, 176.4 and 192kHz

- (optionally, Dolby Digital (AC-3) at 44.1 and 48kHz)

Sink DUTs capable of receiving audio are tested using an Audio/Video Protocol Generator.

Recommended Test Equipment

The recommended Audio/Video Protocol Generator consists of the following components:

- Tektronix DTG5274 Digital Pattern/Timing Generator
- Tektronix DTGM30 (3pcs) output module for DTG5274
- TPA-P-TDR (in some test configurations, where driving a Sink directly)
- SMA Cables as needed to connect output of equipment to TPA boards

5 Tests – Cable Assembly

Due to the difficulty of accessing the plug contacts directly, cable assembly tests may be performed using standard HDMI receptacles, at test points CTP1 and CTP2 shown in Figure 5-1 (corresponding to TP3 and TP4 as used in the HDMI Specification).

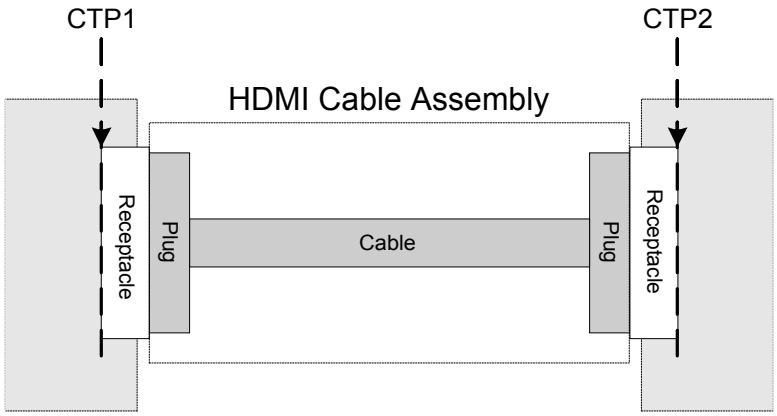


Figure 5-1 Cable Test Points

5.1 Cable – Mechanical

Test ID 5-1: Connector Minimum Envelope

Reference	Requirement
[HDMI: 4.1.9] Connector Drawings	<See reference for details.>

Test Objective

Verify that DUT's connector shell and cable fit inside minimum allowable receptacle envelope.

Required Test Method

- Measure all overmold dimensions.
- [Verify that all dimension fall within maximum permitted values]:
  - If overmold extends more than 3.5mm above or below connector shell → FAIL
  - if overmold extends more than 3.5mm to the left or right of the shell → FAIL
  - if overmold is closer than 9mm to the tip of the shell → FAIL

Recommended Test Method

Perform steps in Required Test Method above using a ruler, caliper, micrometer or similar.

5.2 Cable – Electrical : Required Tests

Test ID 5-2: Wire Assignment

Reference	Requirement
[HDMI: Table 4-8] Type A-to-Type A Cable Wire Assignment	Wire assignment of Type A→Type A cable assembly
[HDMI: Table 4-9] Type A-to-Type B Cable Wire Assignment	Wire assignment of Type A→Type B cable assembly
[HDMI: Table 4-10] Type B-to-Type B Cable Wire Assignment	Wire assignment of Type B→Type B cable assembly

Test Objective

Verify that all specified connections are present in cable and that no connections are present where not specified.

Required Test Method

Refer to one connector as “Connector 1” and the other as “Connector 2”.

Using the appropriate reference for the type of cable tested (Type A vs. Type B connectors) perform the following:

- For each pin “X” from 1 to 19 (if Type A) or 29 (if Type B) on connector 1:
  - For each pin “Y” from 1 to 19 (if Type A) or 29 (if Type B) on connector 2:
    - check connection between Connector 1 pin X and Connector 2 pin Y
    - if connection is specified between Connector 1 pin X and Connector 2 pin Y and no valid connection, → FAIL
    - if no connection is specified between Connector 1 pin X and Connector 2 pin Y and not a valid no-connect, → FAIL
- If cable has Type A connector on one end and Type B on other end:
  - For each pin “X” from 13 to 21, 23 and 24 on Type B connector:
    - For each pin “Y” from X+1 to pin 24 on Type B connector:
      - check connection between pin X and pin Y
      - if connection exists between pin X and pin Y → FAIL

Recommended Test Method

If CDF field Cable_Wire == 'Y' and Cable_Unidirectional == 'N' then the following Recommended Test Method may be used.

A valid connection is defined as <100ohms. For all signal types, a valid no-connect is defined as >1Mohms.

Perform the "Required Test Method" using a standard Digital Multi-meter set for measurement of Resistance using the valid connection criteria above.

Test ID 5-3: TMDS Data Eye Diagram

Reference	Requirement
[HDMI: 4.2.6] Cable Assembly	"An HDMI cable assembly shall produce a TMDS output waveform that meets the Sink eye diagram mask…"
[HDMI: Figure 4-14] Eye Diagram Mask at TP2	The Cable Assembly shall output a data eye compliant with Figure 4-14.

Test Objective

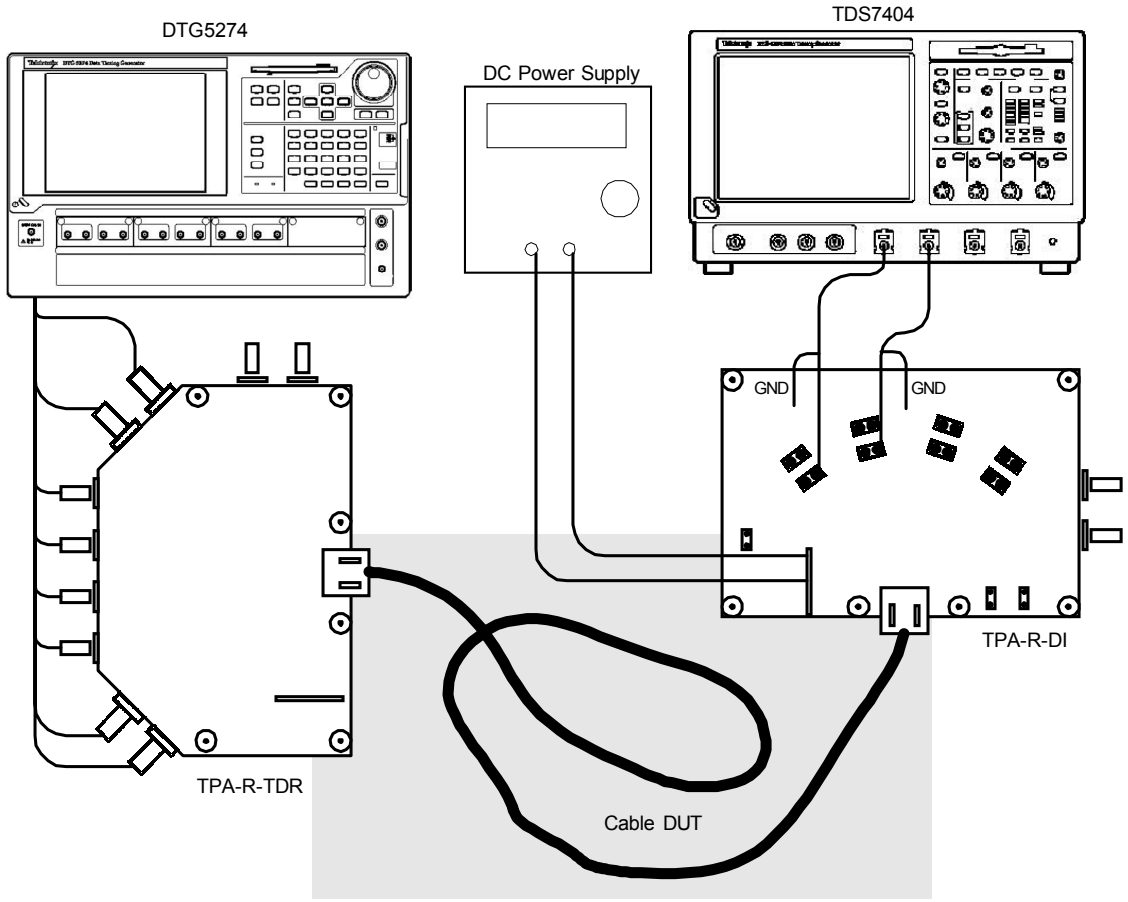
Confirm that the Cable Assembly outputs a compliant data eye.

Required Test Method

All cables must be capable of passing this test. However, for self-testing, this test may be skipped if all of the tests in Section 5.3 Cable – Electrical : Optional (Parametric) Tests, have passed.

- Transmit a video format to the DUT corresponding to the specified bandwidth of the cable. If no bandwidth is specified, transmit a supported format with a 74.25MHz pixel clock.
  - The ATC is not required to test the cable at frequencies higher than 74.25MHz.
- Configure TMDS Signal Generator to output a worst-case eye
- Measure eye at TPA-R-DI (procedure same as Source Eye measurement)
- Measure eye mask on all TMDS_DATA channels at end of cable
- If any measured eyes do not meet the Sink minimum eye mask → FAIL

Recommended Test Method Test ID 5-3: TMDS Data Eye Diagram



Setup 1. Test ID 5-3: TMDS Data Eye Diagram

No.	Description	Recommended TE	Reference	Qty.
1	4GHz Digital Oscilloscope	Tektronix TDS7404	4.2.1.3	1
2	Differential Probes	Tektronix P7330	4.2.1.4	2
3	Digital Timing Generator (DTG)	Tektronix DTG5274	4.2.1.2	1
4	Software CRU	Tektronix SoftCRU	4.2.1.2	1
5	DC Power Supply 3.3V	KENWOOD PW18-1.8AQ	4.2.1.14	1
6	SMA Cables	<See reference>	4.2.1.6	8
7	TPA-R-DI Fixture	Tektronix TPA-R-DI	4.2.1.1.3	1
8	TPA-R-TDR Fixture	Tektronix TPA-R-TDR	4.2.1.1.7	1

- Connect DTG to “input” TPA-P-TDR using eight 1 meter (preferable) or 1.5 meter SMA cables:
  - Module A, Channel 1+, 1-: No connect
  - Module A, Channel 2+, 2-: No connect
  - Module B, Channel 1+, 1-: connect to TMDS_DATA0+, – (“DATA0_P”, “DATA1_N”)
  - Module B, Channel 2+, 2-: connect to TMDS_DATA1+, –
  - Module C, Channel 1+, 1-: connect to TMDS_DATA2+, –
  - Module C, Channel 2+, 2-: connect to TMDS_CLOCK+, –
- Connect Oscilloscope to “output” TPA-R-DI adapter using two Differential Probes, and supply 3.3V power.
- Connect Cable DUT between TPA-R-TDR and TPA-R-DI adapters.
- Configure DTG to output a video format corresponding to the specified bandwidth of the cable. If no bandwidth is specified, configure DTG to output 1920x1080i @ 60Hz (74.25MHz pixel clock).
  - The ATC is not required to test the cable at frequencies higher than 74.25MHz.
- Configure DTG to output worst-case eye as follows:
  - Adjust jitter on TMDS_CLOCK pair to output 0.4nS at 500KHz (worst jitter permitted at TP1= 0.3*T_{BIT} at 75MHz)
  - Adjust output swing voltage to 500mV for every TMDS single-ended signal.
  - Using Jitter/Eye Analyzer, measure TMDS_CLOCK jitter and eye diagram of all three TMDS_DATA pairs
  - Repeat and re-adjust as necessary to create the input worst-case eye diagram
- Measure jitter at TPA-R-DI (procedure same as Source Eye measurement)
- * Measurement BOX vertical setting : Vcenter = (VH + VL) / 2 = ±5mV
- Measure jitter at TPA-R-DI
- If data jitter > 0.67nS (= 0.5*T_{BIT} at 75MHz), then FAIL.
- Adjust DTG swing voltage to (VH, VL)=(3.3V, 2.9V) without jitter.
- Measure eye mask on all TMDS_DATA channels at CTP2
- If any measured eyes do not meet the Sink minimum eye mask → FAIL

5.3 Cable – Electrical : Optional (Parametric) Tests

The tests in this section correspond to the recommended parametric performance of the cable specified in [HDMI: Table 4-18] “Cable Assembly Parameters”. These tests are recommended but not required.

The ATC is not required to perform these tests.

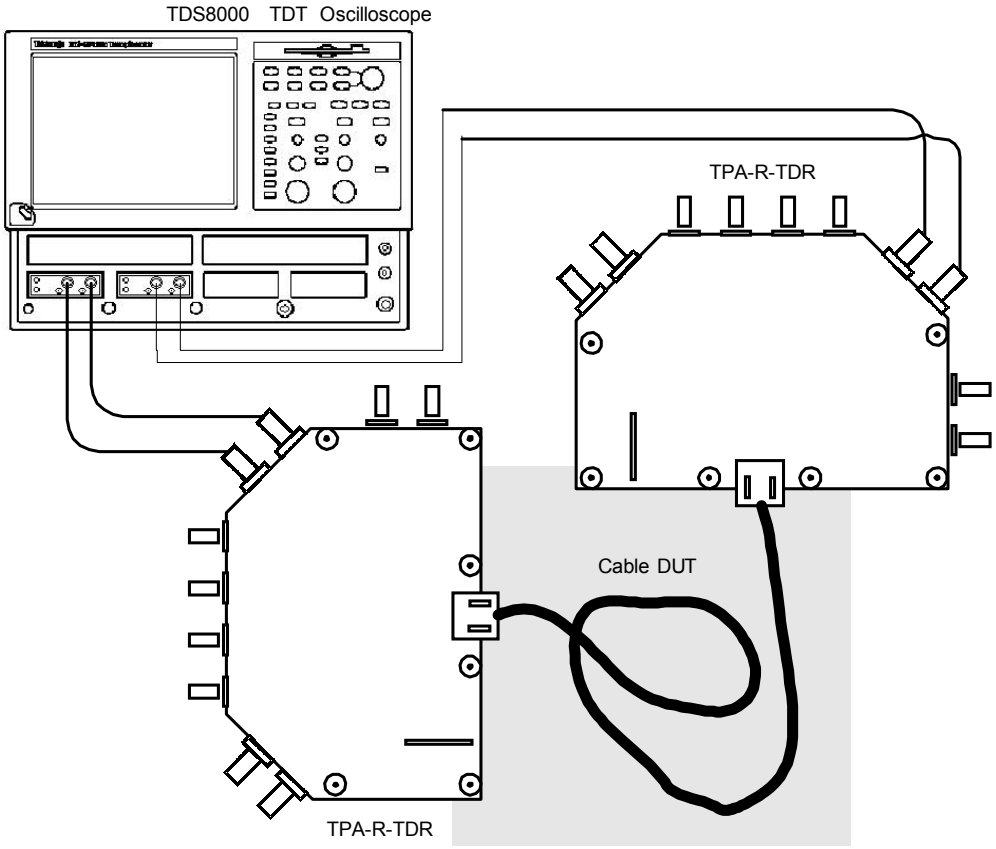
Test ID 5-4: Intra-Pair Skew

Reference	Requirement
[HDMI: 4.2.6] Cable Assembly	“A cable should meet the specifications shown in Table 4-18”
[HDMI: Table 4-18] Cable Assembly Parameters	Cable Assembly Intra-Pair Skew should be no more than 151ps.

Test Objective

Confirm that the Cable Assembly does not have intra-pair skew on the TMDS lines greater than that allowed in the specification.

Recommended Test Method Test ID 5-4: Intra-Pair Skew



Setup 2. Test ID 5-4: Intra-Pair Skew

No.	Description	Recommended TE	Reference	Qty.
1	TDR/TDT Oscilloscope	Tektronix TDS8000B	4.2.1.10	1
2	SMA Cables	<See reference>	4.2.1.6	4
3	TPA-R-TDR Fixture	Tektronix TPA-R-TDR	4.2.1.1.7	2

- De-skew the measurement equipment according to the manufacturer's recommended procedure.
- Connect one TPA-R-TDR adapter to each end of Cable DUT.
- Connect operator to anti-static strap.
- Connect TDT channel #1 to TMDS_DATA0+ and TMDS_DATA0- pins of input TPA-R adapter.
- Connect TDT channel #2 to TMDS_DATA0+ and TMDS_DATA0- pins of output TPA-R adapter.

- Configure TDT to measure the two single-ended signals on channel #2.
- Set vertical axis to 100 mV/Div and horizontal axis to 100 psec/Div.
- Measure skew (delay between inputs on channel 2), T_{IPSKEW}, using TDT oscilloscope. Measurement point is absolute voltage +125mV of Ch3 and -125mV of Ch4.
- If (T_{IPSKEW} > 151ps) then FAIL.
- Repeat the test on the remaining TMDS pairs.

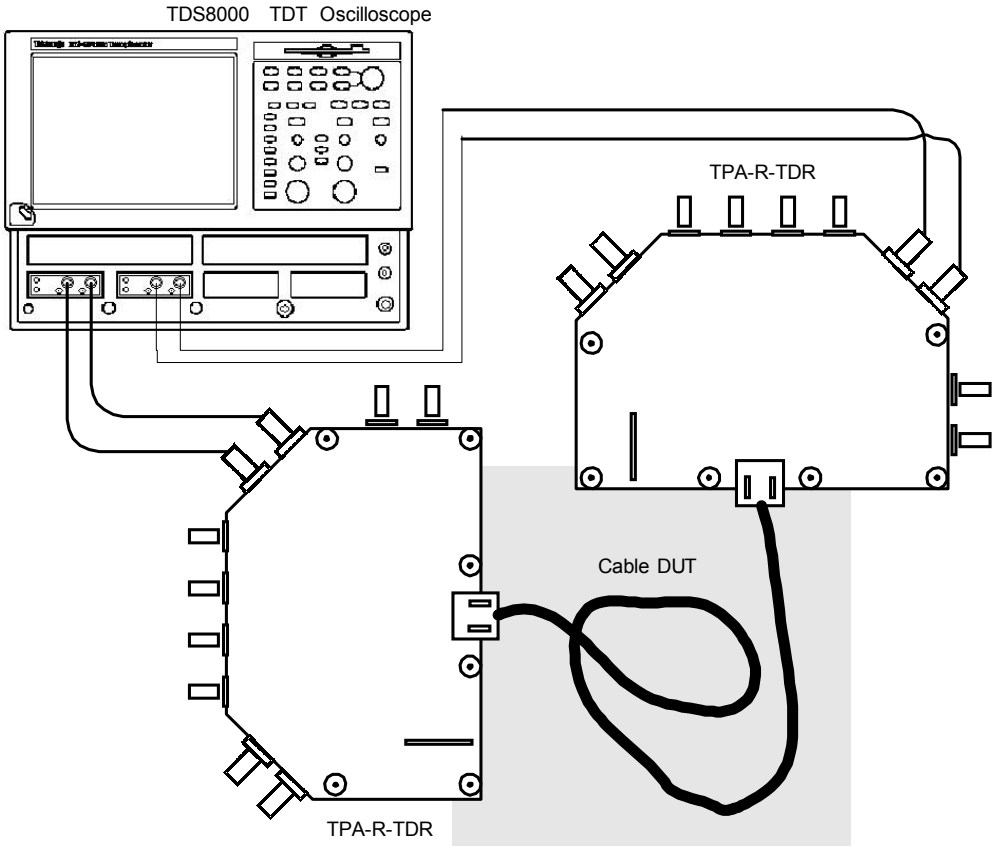
Test ID 5-5: Inter-Pair Skew

Reference	Requirement
[HDMI: 4.2.6] Cable Assembly	”A cable should meet the specifications shown in Table 4-18”
[HDMI: Table 4-18] Cable Assembly Parameters	Cable Assembly Inter-Pair Skew should be no more than 2.42ns

Test Objective

Confirm that the Cable Assembly does not have inter-pair skew on the TMDS lines greater than that allowed in the specification.

Recommended Test Method Test ID 5-5: Inter-Pair Skew



Setup 3. Test ID 5-5: Inter-Pair Skew

No.	Description	Recommended TE	Reference	Qty.
1	TDR/TDT Oscilloscope	Tektronix TDS8000B	4.2.1.10	1
2	SMA Cables	<See reference>	4.2.1.6	4
3	TPA-R-TDR Fixture	Tektronix TPA-R-TDR	4.2.1.1.7	2

- De-skew the measurement equipment according to the manufacturer's recommended procedure
- Connect one TPA-R-TDR adapter to each end of Cable DUT.
- Set vertical axis to 100 mV/Div and horizontal axis to 100 psec/Div.
- Connect SMA cables to TDT Ch1-Ch4
- Configure TDT to measure the differential signal across channel #2.
- For each TMDS differential pair (TMDS_CLOCK, DATA0, DATA1…) perform the following:
  - Connect TDT channel #1 to + and - pins of tested TMDS pair on input TPA-R adapter.
  - Connect TDT channel #2 to + and - pins of tested TMDS pair on output TPA-R adapter.

  - Measure the waveform and save for later analysis.
- Inter-pair Skew measurement point must be 50% of the amplitude of the driven step pulse (e.g. 250mV for the TDS8000B).
- Measure skew (delay between saved waveforms), T_{XPSKEW}, for every combination of channels. This can be done in one operation by overlaying waveforms and noting left-most and right-most edges.
- If (T_{XPSKEW} > 2.42ns) → FAIL

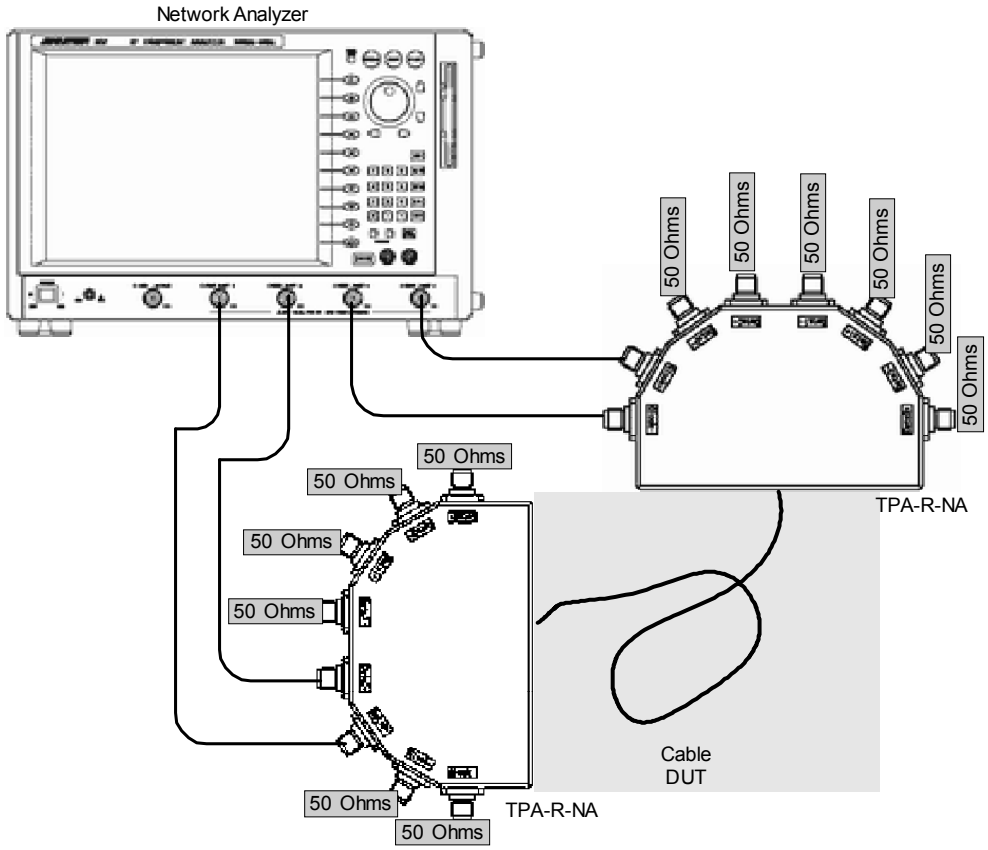
Test ID 5-6: Far End Crosstalk

Reference	Requirement
[HDMI: 4.2.6] Cable Assembly	”A cable should meet the specifications shown in Table 4-18”
[HDMI: Table 4-18] Cable Assembly Parameters	Cable Assembly far end crosstalk should be less than –26dB.

Test Objective

Confirm that the Cable Assembly does not have crosstalk at the far-end between the TMDS lines greater than that allowed in the specification.

Recommended Test Method Test ID 5-6: Far End Crosstalk



Setup 4. Test ID 5-6: Far End Crosstalk

No.	Description	Recommended TE	Reference	Qty.
1	Network Analyzer (NA)	ADVANTEST R3860	4.2.1.9	1
2	SMA Cables	<See reference>	4.2.1.6	4
3	50 Ohm SMA Terminators	<See reference>	4.2.1.7	12
4	TPA-R-NA Fixture	ADVANTEST CAX-ATI013	4.2.1.1.8	2

- Setup the ADVANTEST analyzer with 1601 measurement points, measurement frequency range of 300kHZ to 5GHz. IF bandwidth is not critical.
- Calibrate the NA using a 4-port auto-calibration kit, or a standard calibration kit.
- Calibrate NA, including SMA and TPA fixture, using a port extension function. Less than ±10 degrees at 2.475GHz.
- Connect input end of cable to first TPA-R adapter.
- Connect output end of cable to second TPA-R adapter.
- Connect Network Analyzer ports 1 and 2 to the input TPA-R fixture, TMDS_CLOCK channel + and – respectively.

- Connect Network Analyzer ports 3 and 4 to the output TPA fixture, TMDS_DATA0 + and – respectively.
- Connect a 50-ohm terminator to each of the untested TMDS signals.
- Measure the crosstalk and find the maximum value (X_{FE})
- If $X_{FE} \geq$ -26dB then FAIL.
- Repeat the measurement for all remaining combinations of TMDS pairs.

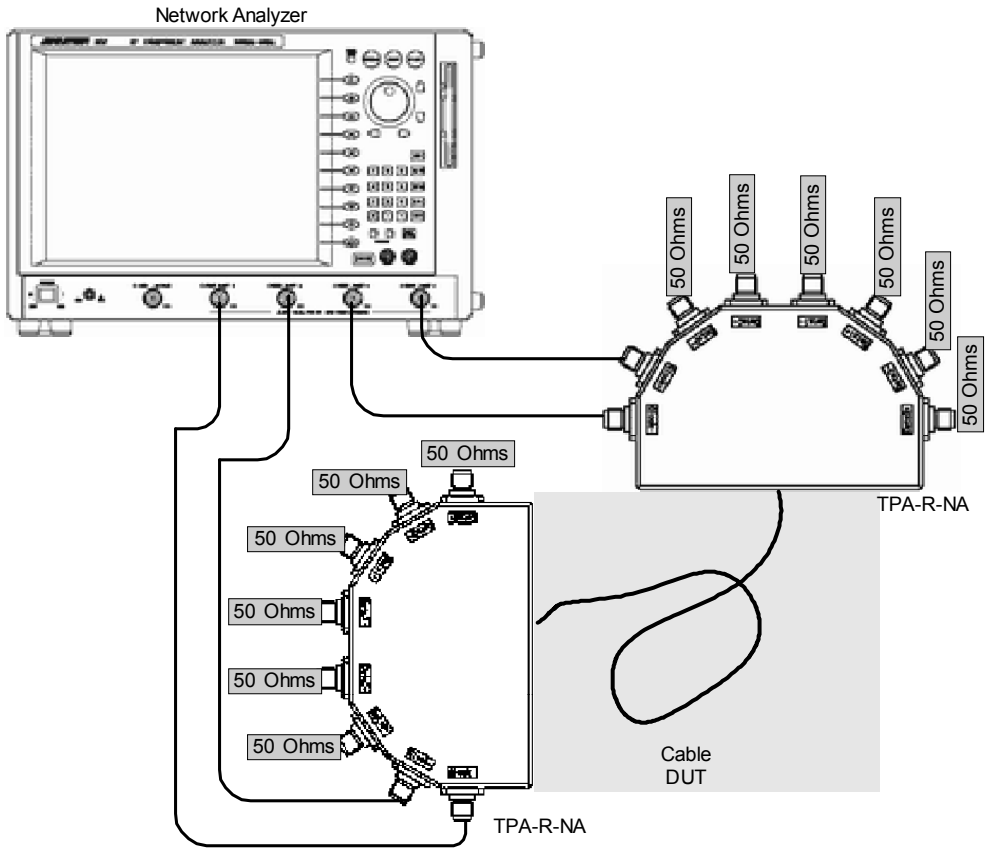
Test ID 5-7: Attenuation

Reference	Requirement
[HDMI: 4.2.6] Cable Assembly	”A cable should meet the specifications shown in Table 4-18”
[HDMI: Table 4-18] Cable Assembly Parameters	Maximum allowed Cable Assembly attenuation shall be: for 300kHz – 825MHz … 8dB for 825MHz – 2.475GHz … 21dB for 2.475GHz – 4.125GHz … 30dB

Test Objective

Confirm that the Cable Assembly does not have attenuation on the TMDS lines greater than that allowed in the specification.

Recommended Test Method Test ID 5-7: Attenuation



Setup 5. Test ID 5-7: Attenuation

No.	Description	Recommended TE	Reference	Qty.
1	Network Analyzer (NA)	ADVANTEST R3860	4.2.1.9	1
2	SMA Cables	<See reference>	4.2.1.6	4
3	50 Ohm SMA Terminators	<See reference>	4.2.1.7	12
3	TPA-R-NA Fixture	ADVANTEST CAX-ATI013	4.2.1.1.8	2

- Connect input end of cable to first TPA-R-NA adapter.
- Connect output end of cable to second TPA-R-NA adapter.
- Setup the ADVANTEST analyzer with 1601 measurement points, measurement frequency range of 300kHz to 5GHz. IF bandwidth is not critical.
- Calibrate the NA using a 4-port auto-calibration kit, or a standard calibration kit.
- Calibrate NA, including SMA and TPA fixture, using a port extension function. Less than ±10 degrees at 2.475GHz.
- Connect Network Analyzer ports 1 and 2 to the input TPA fixture, TMDS Clock channel '+' and '–' respectively.

- Connect Network Analyzer ports 3 and 4 to the output TPA fixture, TMDS Clock channel '+' and '–' respectively.
- Connect a 50-ohm terminator to each of the untested TMDS signals.
- Measure the attenuation using SDD21 log-mag (S-parameter, S-matrix component number 2-1, differential-to-differential).
- For the measured attenuation, A:
  - If (A > 8dB) in the range 300kHz to 825MHz then FAIL.
  - If (A > 21dB) in the range 825MHz to 2.475GHz then FAIL.
  - If (A > 30dB) in the range 2.475GHz to 4.125GHz then FAIL.
- Repeat the measurement for remaining TMDS channels.

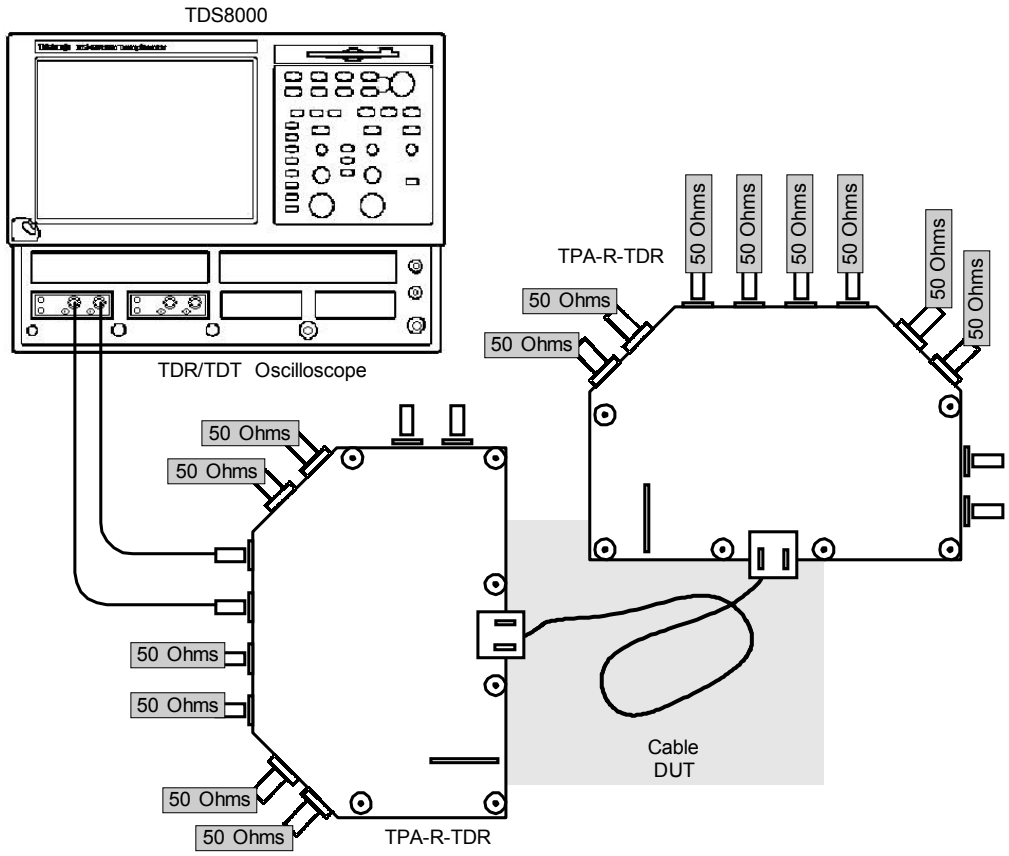
Test ID 5-8: Differential Impedance

Reference	Requirement
[HDMI: 4.2.6] Cable Assembly	”A cable should meet the specifications shown in Table 4-18”
[HDMI: Table 4-18] Cable Assembly Parameters	Cable Assembly differential impedance should be: 100Ω±15%, measured at connector area, and 100Ω±10%, measured at the cable area.

Test Objective

Confirm that the Cable Assembly does not have differential impedance on the TMDS lines outside the tolerances allowed in the specification.

Recommended Test Method Test ID 5-8: Differential Impedance



Setup 6. Test ID 5-8: Differential Impedance

No.	Description	Recommended TE	Reference	Qty.
1	TDR/TDT Oscilloscope	Tektronix TDS8000B	4.2.1.10	1
2	SMA Cables	<See reference>	4.2.1.6	2
4	50 Ohm SMA Terminators	<See reference>	4.2.1.7	14
3	TPA-R-TDR Fixture	Tektronix TPA-R-TDR	4.2.1.1.7	2

- Connect near end of cable to first TPA-R-TDR adapter.
- Connect far end of cable to second TPA-R-TDR adapter.
- Connect 50 ohm terminators to all TMDS + and – signals on the far-end TPA-R.
- Connect SMA cable from TDR oscilloscope to TMDS_DATA0+ on near-end TPA-R.
- Connect 50 ohm terminators to all untested TMDS signals on near-end TPA-R.
- Configure the TDR oscilloscope to measure differential impedance in TDR mode:
  - TDR rise time = 200ps (determined by using the test coupon on TPA-R, if available)
  - Vertical axis set to ‘ohms’.

- View the TDR trace of impedance, Z_{DIFF}, on TMDS_DATA0+:
  - Through the connector and transition area, if (Z_{DIFF} < 85 Ω) OR (Z_{DIFF} > 115 Ω) then FAIL.
  - In cable area, if (Z_{DIFF} < 90 Ω) OR (Z_{DIFF} > 110 Ω) then FAIL.
- Repeat the test for all remaining + and - TMDS signals.

6 Tests – Plug and Receptacle

The following tests must be run on individual connector samples at a facility equipped for such testing. The adopter may have this testing performed by the supplier of the connector. All HDMI connectors on Cable Assemblies, Sources, Sinks and Repeaters shall be capable of passing all of the tests in this section.

6.1 Mechanical Tests

Test ID 6-1: Connector Mechanical Specification

Reference	Requirement
[HDMI: 4.1.5] Connector Drawings	<See reference for details.>

Test Objective

Verify that plug mechanical dimensions are within specified tolerances.

Required Test Method

- Measure the following dimensions: all mating surfaces of shell, pins.
- Connector dimensions shall be within tolerances shown in relevant figures. [HDMI: Figure 4-1 through Figure 4-6]

Recommended Test Method

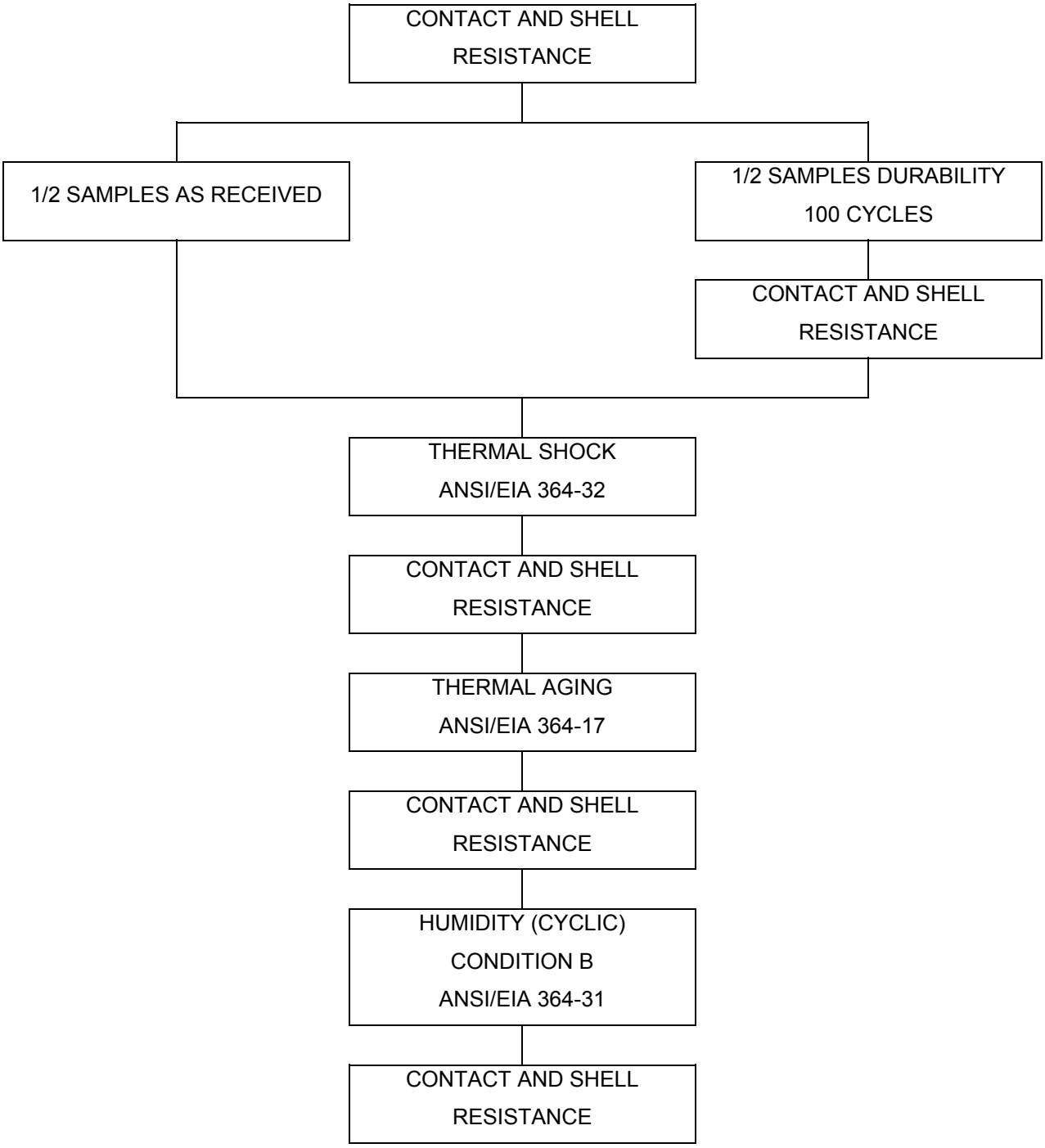
Perform steps in Required Test Method above.

6.2 Connector – ANSI 364 Tests

Tested using ANSI/EIA 364. Refer to [HDMI: 4.1.6, 4.1.7 and 4.1.8] for parameter to be measured.

Reference	Requirement
ANSI/EIA 364	<See reference for details.>
[HDMI: 4.1.6, 4.1.7 and 4.1.8]	<See reference for details.>

Test ID 6-2: GROUP1: Environmental Performance

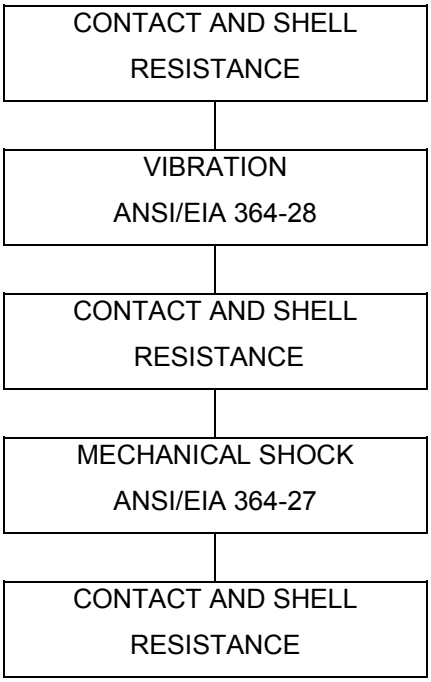


Number of Samples

6 : Receptacle assembled to printed circuit board.

6 : Cable assemblies with a plug assembled to one end, 50.8mm long.

Test ID 6-3: GROUP2: Mated Mechanical

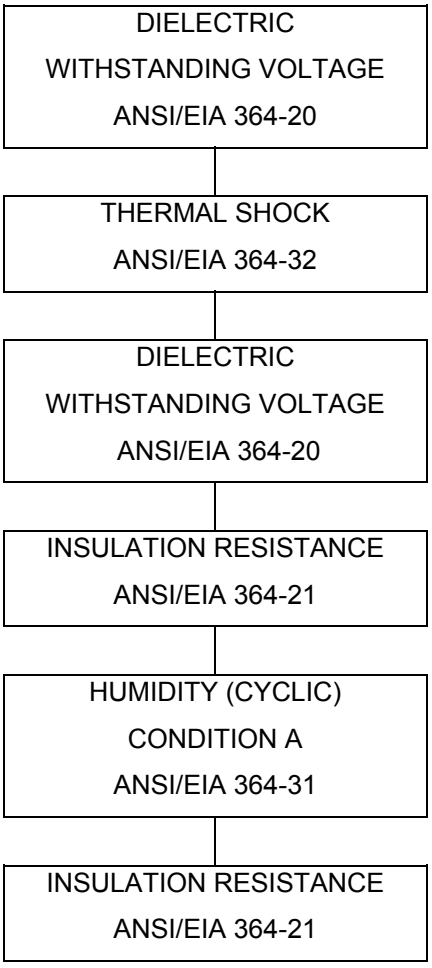


Number of Samples

2 : Receptacle assembled to printed circuit board.

2 : Cable assemblies with a plug assembled to one end, 50.8mm long.

Test ID 6-4: GROUP 3 Insulator Integrity

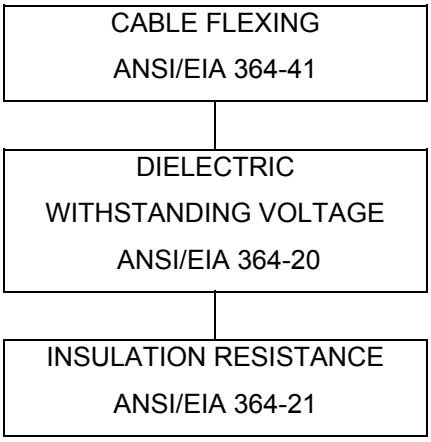


Number of Samples

2 : Receptacle assembled to printed circuit board.

2 : Cable assemblies with a plug assembled to one end, 50.8mm long.

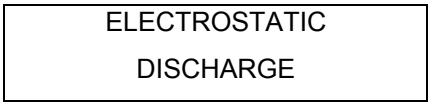
Test ID 6-5: GROUP 4 Cable Flexing



Number of Samples

2 : Cable assemblies.

Test ID 6-6: GROUP 5 Electrostatic Discharge



Number of Samples

1 : Receptacle connector.

1 : Plug Cable

7 Tests – Source

7.1 Source Products Overview

In order to be adequately tested, the Source (DUT) shall have the ability to output an HDMI signal that is indicative of the behavior of the Source DUT during normal user operation. For instance,

- If the DUT is a DVD player or similar device, the operator may use the ability of the DUT to playback pre-recorded or recorded media (disk, tape, etc) in order to output the HDMI video test signal.
- If the DUT is a set-top box or similar device, the operator may use the ability of the DUT to decode a received signal in order to output the HDMI video test signal.
- The operator may use a menu mode or other user interface on the DUT in order to output an HDMI signal.

The Source device needs to output an HDMI signal as specified in the test. This procedure will be product-specific but will likely be accomplished by presenting specific EDID images to the Source, manually configuring the Source and/or by supplying certain media or content into the Source. In many cases, this effort can be assisted by configuring an EDID present in the test equipment (analyzer) to indicate support for each of the formats supported by the Source.

7.2 Source – EDID / E-DDC / HPD

Test ID 7-1: EDID-Related Behavior

Reference	Requirement
[HDMI: 8.4.5] Enhanced DDC Source	"The Source shall use Enhanced DDC protocols. The Source reads Enhanced EDID extensions data at DDC address 0xA0 using segment pointer 0x60."
[HDMI: 8.3] EDID Data Structure	"A Source shall read the EDID 1.3 and first CEA EDID Timing Extension to determine the capabilities supported by the Sink."

Test Objective

Verify that Source supports the reading of a 4-block EDID using the E-DDC segment pointer.

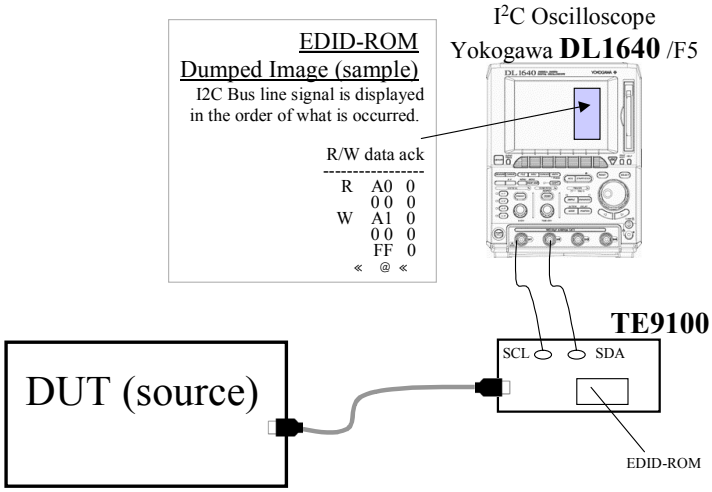
Required Test Method

- Attach Source DUT to EDID Emulator.
- Attach I^2C Analyzer to SDA and SCL signals on EDID Emulator.
- Turn on Source DUT
- Configure I^2C Analyzer to capture and analyze all I^2C transactions.
- Configure EDID Emulator for 750pF total capacitance (emulator plus cable) and nominal pull-up resistance on SDA and SCL.

- Apply a valid HDMI EDID containing the following 2 blocks:
  - 0: EDID 1.3
    1: CEA Timing Extension version 3
- Pulse HPD for more than 100msec
- Examine I^2C transactions occurring after HPD pulse.
- If I^2C commands do not perform full read of EDID blocks 0 and 1 → FAIL
  (Note: There should be no attempt to verify that the DUT has successfully captured the data, only that the appropriate transaction occur.)

- Apply a valid HDMI EDID containing the following 4 blocks:
  - 0: EDID 1.3
    1: Extension Map
    2: CEA Timing Extension version 3 (includes HDMI VSDB)
    3: CEA Timing Extension version 3 (single DTD)
- Pulse HPD for more than 100msec
- Examine I^2C transactions occurring after HPD pulse.
- If I^2C commands do not perform full read of EDID blocks 0, 1 and 2 → FAIL

Recommended Test Method Test ID 7-1: EDID-Related Behavior



No.	Description	Recommended TE	Reference	Qty.
1	I^2C Analyzer	Yokogawa DL1640	4.2.3.3	1
2	DC Power Supply 3.3V	KENWOOD PW18-1.8AQ	4.2.1.14	1
3	EDID Emulator	Silicon Image TE9100	4.2.3.2	1

- Attach Source DUT to EDID Emulator using a short (<1meter) HDMI cable.
- Connect probes of Yokogawa DL1640 to SDA and SCL signals on EDID Emulator.
- Turn on Source DUT
- Configure oscilloscope:
  - I^2C mode is selected
  - Trigger is set to “Single shot” mode.
  - Triggering pattern is set to “address = 0xA0”.
- Configure I^2C Analyzer to capture and analyze all I^2C transactions.
- Configure EDID Emulator capacitance so that total capacitance of Emulator and HDMI cable is 750pF. Configure EDID Emulator to have nominal pull-up resistance on SDA and SCL.

- Apply a valid HDMI EDID containing the following 2 blocks:
  - 0: EDID 1.3
    1: CEA Timing Extension version 3
- Pulse HPD for more than 100msec
- If no oscilloscope trigger occurs → FAIL
- If oscilloscope capture does not contain: <0xA0+ack> <0x00+ack> RS <0xA1+ack> → FAIL

- If I^2C commands do not perform full read of EDID blocks 0 and 1 → FAIL
  (Note: there should be no attempt to verify that DUT has successfully captured the data.)

- Apply a valid HDMI EDID containing the following 4 blocks:
  - 0: EDID 1.3
    1: Extension Map
    2: CEA Timing Extension version 3 (includes HDMI VSDB)
    3: CEA Timing Extension version 3 (single DTD)
- Pulse HPD for more than 100msec
- If no oscilloscope trigger occurs → FAIL
- If oscilloscope capture does not contain: <0x60+ack> <0x01+ack> RS <0xA0+ack> → FAIL
- If I^2C commands do not perform full read of EDID blocks 0, 1 and 2 → FAIL

7.3 Source – Electrical

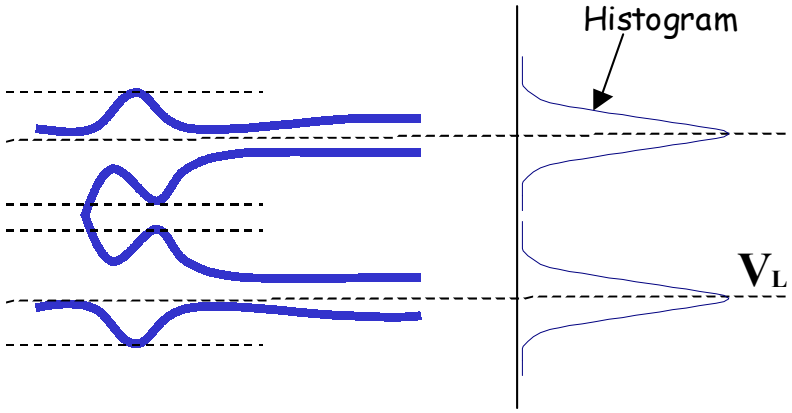
Test ID 7-2: TMDS –V_L

Reference	Requirement
[HDMI: 4.2.4] HDMI Source TMDS Characteristics	"The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals."
[HDMI: Table 4-12] Source DC Characteristics at TP1	Single-ended low level output voltage, V_L: $(AV_{CC}\text{-}600mV) \le V_L \le (AV_{CC}\text{ -}400mV)$

Test Objective

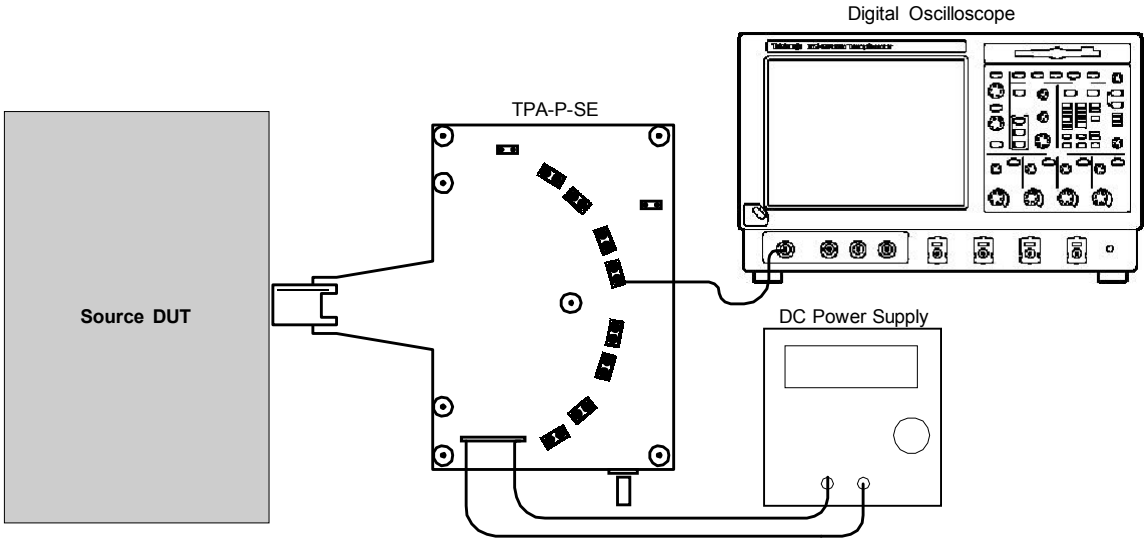
Confirm that DC voltage levels on the HDMI link are within specified limits for each TMDS signal.

Required Test Method



- Connect TPA-P-SE adapter to Source DUT HDMI output connector.
- Control the Source DUT to output a video format with lowest supported pixel clock frequency.
- Connect probe to TMDS_DATA0+.
- Capture 10,000 repetitions
- Measure low voltage (V_L) using Histogram Method (described below).
- If (V_L > 2.900V) OR (V_L < 2.700V) then FAIL
- Repeat steps for all remaining TMDS clock and data signals.

Recommended Test Method Test ID 7-2: TMDS –VL



Setup 7. Test ID 7-2: TMDS –VL

No.	Description	Recommended TE	Reference	Qty.
1	4GHz Digital Oscilloscope	Tektronix TDS7404	4.2.1.3	1
2	Single-Ended Probe	Tektronix P7240	4.2.1.5	1
3	DC Power Supply 3.3V	KENWOOD PW18-1.8AQ	4.2.1.14	1
4	EDID Emulator	Silicon Image TE9100	4.2.3.2	1
5	TPA-P-SE Fixture	Tektronix TPA-P-SE	4.2.1.1.4	1

- Note that V_L is specified as a DC characteristics and as such is impossible to measure on an active TMDS signal. Instead, the following procedure measures the most common voltage levels in the low area of the AC waveform.
- Connect TPA-P-SE adapter to Source DUT HDMI output connector.
- Control the Source DUT to output a video format with lowest supported pixel clock frequency.
- Connect probe to TMDS_DATA0+.
- Capture 10,000 repetitions, triggered at mid-point of waveform, of duration ≥ $2*T_{BIT}$ to get proper histograms.

- Display the histogram of vertical frequency of its level on the TDS7404:
  - Measure – Measurement Setup and Setup – “Ref Levs” – “Snapshot”
  - “Determine Base, Top Form” – “Histogram”
- Read the V_L value using the Histogram Method. On the TDS7404:

- Select from the menu [Measure][Amplitude][Low Level] for V_L

- If (V_L > 2.900V) OR (V_L < 2.700V) then FAIL
- Repeat the test for all eight TMDS signals.

Histogram Method requires use of a Digital Oscilloscope to determine the value of V_L. The most common voltage value is the mathematical 'mode' of the set of values collected and is determined from the peak of a histogram measurement of the collected samples.

For example, when collecting 10,000 triggered waveforms, the "peak" or mode voltage value is that voltage value most frequent in the data. This value may be different from the mean and median values. V_H is the mode high level. V_L is the mode low level.

Test ID 7-3: TMDS – I_{OFF}

Reference	Requirement
[HDMI: 4.2.4] HDMI Source TMDS Characteristics	"The Source shall meet the DC specifications in Table 4-12 for all operating conditions specified in Table 4-11 when driving clock and data signals."
[HDMI: Table 4-12] Source DC Characteristics at TP1	TMDS leakage current, I_{OFF} must be less than 10µA.

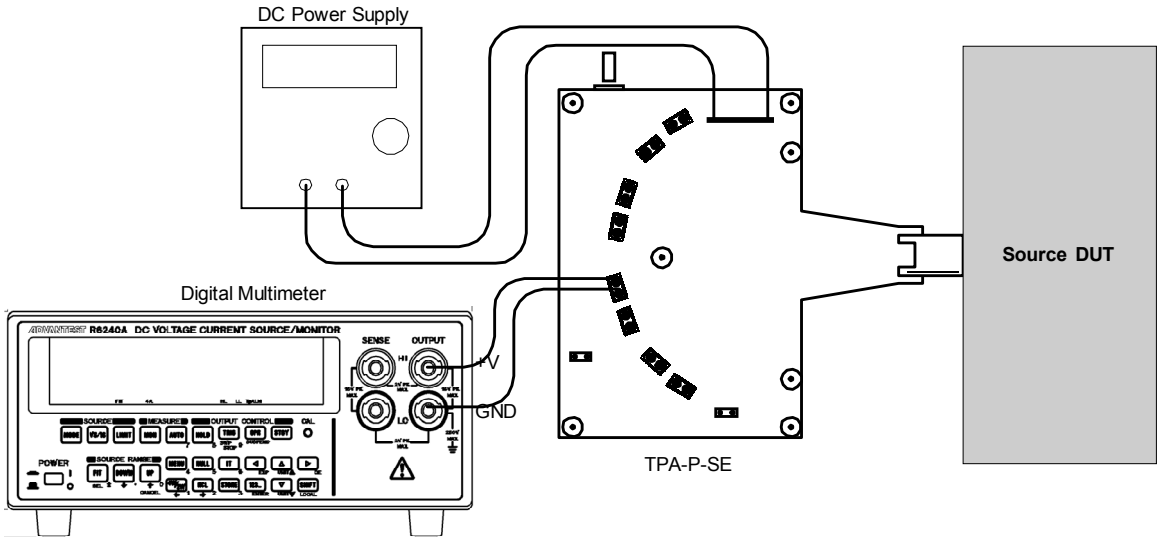
Test Objective

Confirm that a disabled TMDS link allows leakage currents only within specified limits.

Required Test Method

- Connect TPA-P adapter to Source DUT HDMI output connector.
- Configure Source DUT to disable its HDMI output, either by powering off DUT or through other means.
- Measure current, I_{OFF}, on TMDS_DATA0+.
- If I_{OFF} > 10µA then FAIL.
- Repeat test for all remaining TMDS_DATAand TMDS_CLOCK, + and - signals.

Recommended Test Method Test ID 7-3: TMDS – IOFF



Setup 8. Test ID 7-3: TMDS – IOFF

No.	Description	Recommended TE	Reference	Qty.
1	Voltage Meter	ADVANTEST R6552	4.2.1.12	1
2	DC Power Supply 3.3V	KENWOOD PW18-1.8AQ	4.2.1.14	1
3	EDID Emulator	Silicon Image TE9100	4.2.3.2	1
4	TPA-P-SE Fixture	Tektronix TPA-P-SE	4.2.1.1.4	1

Connect TPA-P-SE adapter to Source DUT HDMI output connector.

- Supply 3.3V to the TPA-P-SE adapter. Configure: Each TMDS signal has a 50Ω ± 0.1% pull-up.
- Configure Source DUT to disable its HDMI output, either by powering off DUT or through other means..
- Configure the Voltage Meter to measure voltage.
- Connect Voltage Meter probes across the pull-up resistor on TMDS_DATA0+.
- Measure voltage, V_{50}.
- Calculate $I_{OFF} = V_{50} / 50$ ohms.
- If $I_{OFF} > 10\mu A \rightarrow$ FAIL.
- Repeat measurement for all remaining TMDS Clock and Data, + and - signals.

Test ID 7-4: TMDS – T_{RISE}, T_{FALL}

Reference	Requirement
[HDMI: 4.2.4] HDMI Source TMDS Characteristics	"The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11."
[HDMI: Table 4-13] Source AC Characteristics at TP1	75psec ≤ Rise Time or Fall Time ≤ 0.4*T_{BIT}

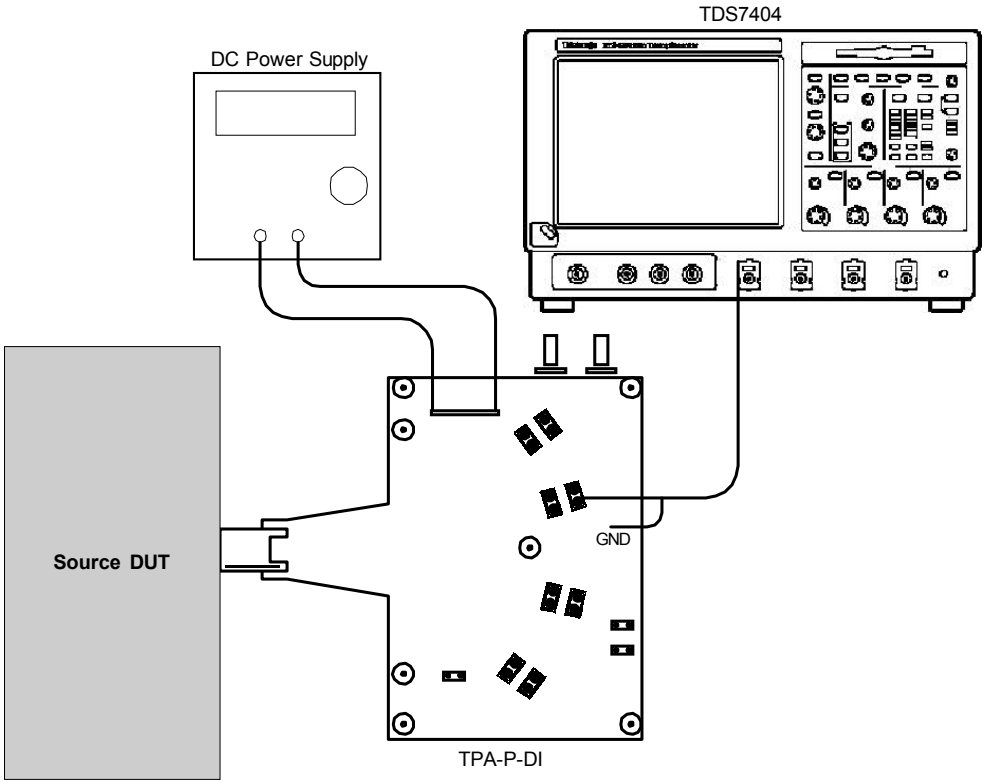
Test Objective

Confirm that the rise times and fall times on the TMDS differential signals fall within the limits of the specification.

Required Test Method

- Connect TPA-P adapter to Source DUT HDMI output connector.
- Configure Source DUT to output a video format with highest supported pixel clock frequency.
- Accumulate at least 10,000 triggered waveforms.
- Measure T_{RISE} as the mode of the sampled edge times from 20% to 80% of the differential swing voltage rising edge.
- Measure T_{FALL} as the mode of the sampled edge times from 80% to 20% of the differential swing voltage on the opposite edge.
- If (T_{RISE} < 75ps) OR (T_{RISE} > 0.4 * T_{BIT}) then FAIL.
- If (T_{FALL} < 75ps) OR (T_{FALL} > 0.4 * T_{BIT}) then FAIL.
- Repeat the test for all remaining TMDS clock and data pairs.

Recommended Test Method Test ID 7-4: TMDS – TRISE, TFALL



Setup 9. Test ID 7-4: TMDS – TRISE, TFALL

No.	Description	Recommended TE	Reference	Qty.
1	4GHz Digital Oscilloscope	Tektronix TDS7404	4.2.1.3	1
2	Differential Probe	Tektronix P7330	4.2.1.4	1
3	DC Power Supply 3.3V	KENWOOD PW18-1.8AQ	4.2.1.14	1
4	EDID Emulator	Silicon Image TE9100	4.2.3.2	1
5	TPA-P-DI Fixture	Tektronix TPA-P-DI	4.2.1.1.2	1

- Connect TPA-P-DI adapter to Source DUT HDMI output connector.
- Connect power supply to TPA board.
- Configure Source DUT to output a video format with highest supported pixel clock frequency.
- Connect differential probe to TMDS_DATA0 and configure as trigger. Position the trigger at the center of the screen.
- Set horizontal range to $2*T_{BIT}$ or more.
- Accumulate at least 10,000 triggered waveforms.

- Measure T_{RISE} from 20% to 80% of the differential swing voltage rising edge. The measurement finds the mode of the rise times measured for each trigger across the set of samples.
- Measure T_{FALL} from 80% to 20% of the differential swing voltage on the opposite edge.
- If (T_{RISE} < 75ps) OR (T_{RISE} > 0.4 * T_{BIT}) then FAIL.
- If (T_{FALL} < 75ps) OR (T_{FALL} > 0.4 * T_{BIT}) then FAIL.
- Repeat the test for all remaining TMDS clock and data pairs.

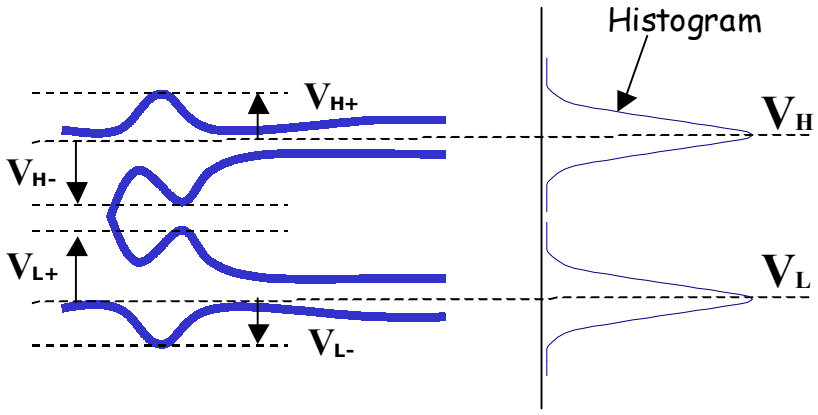
Test ID 7-5: TMDS – Over/Undershoot

Reference	Requirement
[HDMI: 4.2.4] HDMI Source TMDS Characteristics	"The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11."
[HDMI: Table 4-13] Source AC Characteristics at TP1	TMDS overshoot must be ≤15% of $2*V_{SWING}$. TMDS undershoot must be ≤ 25% of $2*V_{SWING}$.

Test Objective

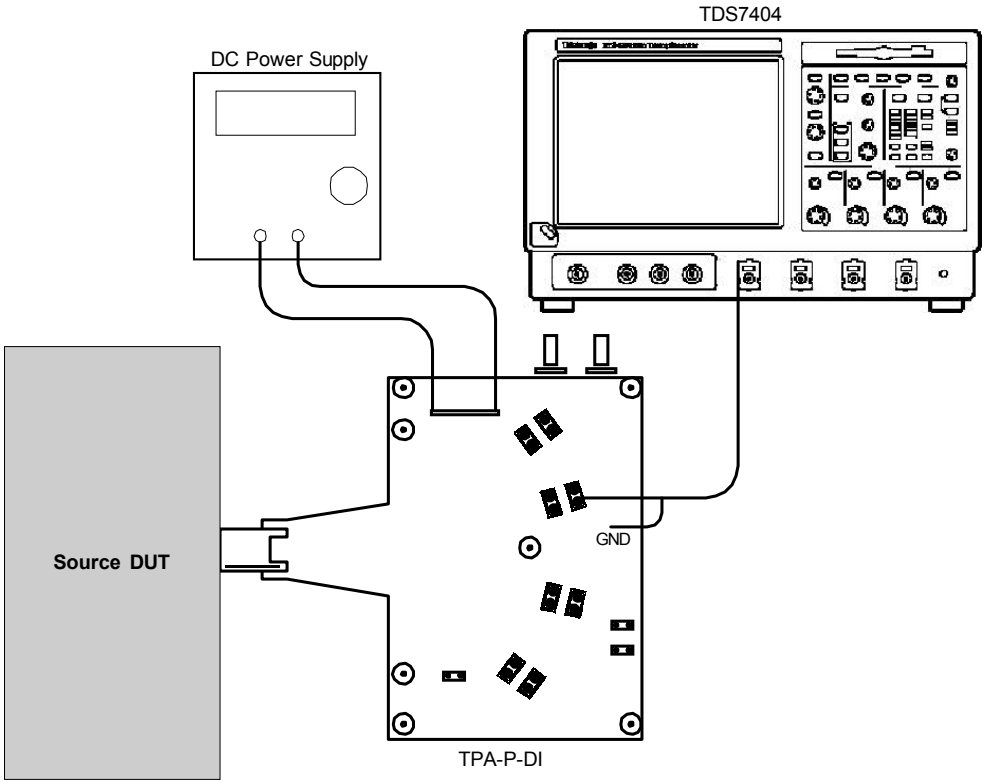
Confirm that the differential TMDS signals do not have overshoot or undershoot beyond that allowed by the specified limits.

Required Test Method



- Connect TPA-P adapter to Source DUT HDMI output connector.
- Control the Source DUT to output a video format with lowest supported pixel clock frequency.
- Connect the differential probe to TMDS_DATA0.
- Set oscilloscope horizontal scale to show at least $2*T_{BIT}$.
- Measure the values V_H, V_L V_H+, V_H-, V_L+ and V_L-, using the Histogram Method.
- Calculate $V_{SWING} = (V_H - V_L)/2$.
- Calculate Overshoot = max{V_H+, V_L-}, and Undershoot = max{V_H-, V_L+}.
- If Overshoot > 15% of $2*V_{SWING}$ then FAIL.
- If Undershoot > 25% of $2*V_{SWING}$ then FAIL.
- Repeat for all remaining TMDS clock and data pairs.

Recommended Test Method Test ID 7-5: TMDS – Over/Undershoot



Setup 10. Test ID 7-5: TMDS – Over/Undershoot

No.	Description	Recommended TE	Reference	Qty.
1	4GHz Digital Oscilloscope	Tektronix TDS7404	4.2.1.3	1
2	Differential Probe	Tektronix P7330	4.2.1.4	1
3	DC Power Supply 3.3V	KENWOOD PW18-1.8AQ	4.2.1.14	1
4	EDID Emulator	Silicon Image TE9100	4.2.3.2	1
5	TPA-P-DI Fixture	Tektronix TPA-P-DI	4.2.1.1.2	1

- Connect TPA-P adapter to Source DUT HDMI output connector.
- Supply 3.3V to the TPA-P-DI adapter.
- Control the Source DUT to output a video format with lowest supported pixel clock frequency.
- Connect the differential probe to TMDS_DATA0.
- Set oscilloscope horizontal scale to show at least 2*T_{BIT}.
- Measure the values V_H, V_L, V_H+, V_H-, V_L+ and V_L-, using the following method.:
- Display the histogram of vertical frequency of its level on the TDS7404:

- Measure – Measurement Setup and Setup – “Ref Levs” – “Snapshot”
- “Determine Base, Top Form” – “Histogram”

- Read the V_H and V_L values using the Histogram Method. On the TDS7404:
- Select from the menu [Measure][Amplitude][High Level] for V_H.
- Select from the menu [Measure][Amplitude][Low Level] for V_L, after readjusting scale.
- Calculate $V_{SWING} = (V_H – V_L)/2$.
- Calculate Overshoot = max{V_H+, V_L-}, and Undershoot = max{V_H-, V_L+}.
- If Overshoot > 15% of $2*V_{SWING}$ then FAIL.
- If Undershoot > 25% of $2*V_{SWING}$ then FAIL.
- Repeat for all remaining TMDS clock and data (+ and -) signals.

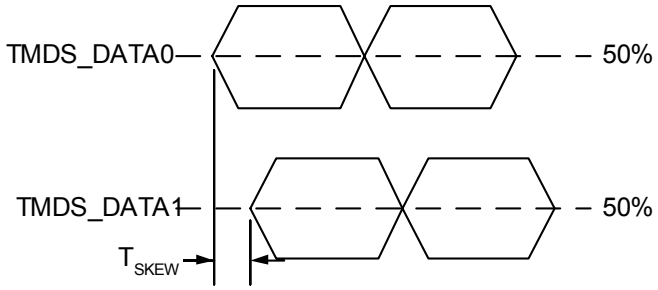
Test ID 7-6: TMDS – Inter-Pair Skew

Reference	Requirement
[HDMI: 4.2.4] HDMI Source TMDS Characteristics	"The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11."
[HDMI: Table 4-13] Source AC Characteristics at TP1	Inter-pair skew must not exceed $0.20*T_{PIXEL}$.

Test Objective

Confirm that any skew between the differential pairs in the TMDS portion of the HDMI link does not exceed the limits in the specification.

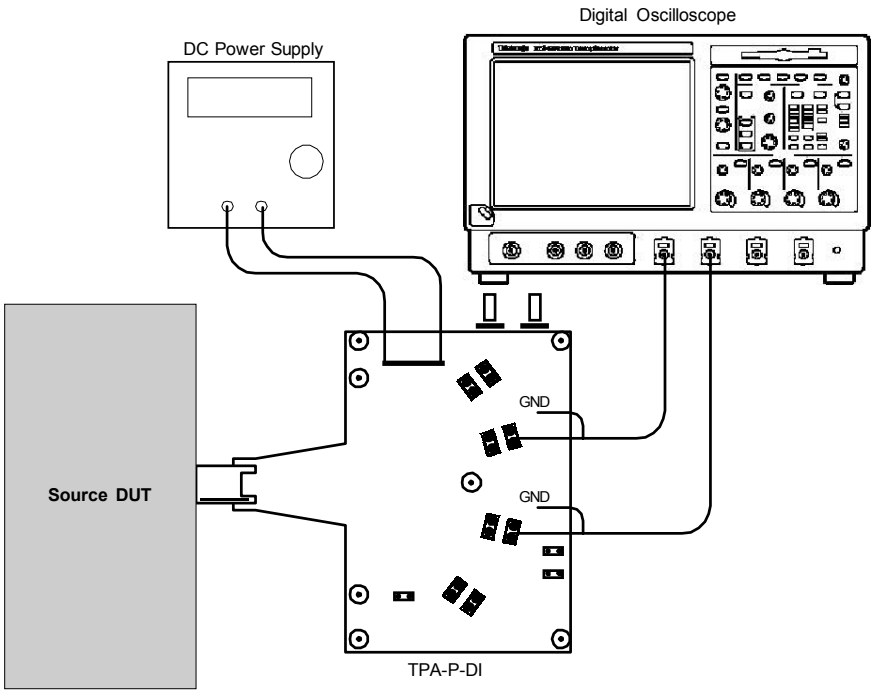
Required Test Method



- Connect TPA-P adapter to Source DUT HDMI output connector.
- Connect first differential probe to TMDS_DATA0.
- Connect second differential probe to TMDS_DATA1.
- Configure Source DUT to output a video format with highest supported pixel clock frequency.
- Measure T_{SKEW}
- If $T_{SKEW} > 0.2*T_{PIXEL}$ then fail.

Repeat the test for remaining combinations of TMDS pairs.

Recommended Test Method Test ID 7-6: TMDS – Inter-Pair Skew



Setup 11. Test ID 7-6: TMDS – Inter-Pair Skew

No.	Description	Recommended TE	Reference	Qty.
1	4GHz Digital Oscilloscope	Tektronix TDS7404	4.2.1.3	1
2	Differential Probe	Tektronix P7330	4.2.1.4	2
3	DC Power Supply 3.3V	KENWOOD PW18-1.8AQ	4.2.1.14	1
4	EDID Emulator	Silicon Image TE9100	4.2.3.2	1
5	TPA-P-DI Fixture	Tektronix TPA-P-DI	4.2.1.1.2	1

- Connect TPA-P-DI adapter to Source DUT HDMI output connector.
- Connect first differential probe to TMDS_DATA0.
- Connect second differential probe to TMDS_DATA1.
- Configure Source DUT to output a video format with highest supported pixel clock frequency.
- Set pattern trigger on first channel with CTL encoding pattern.
- Examine second channel for valid CTL code (or edge if TMDS_CLOCK) and measure T_{IPSKEW} between channels.
- If $T_{SKEW} > 0.2*T_{PIXEL}$ then fail.
- Repeat the test for remaining combinations of TMDS pairs.

Test ID 7-7: TMDS – Intra-Pair Skew

Reference	Requirement
[HDMI: 4.2.4] HDMI Source TMDS Characteristics	"The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11."
[HDMI: Table 4-13] Source AC Characteristics at TP1	Intra-pair skew must not exceed $0.15*T_{BIT}$.

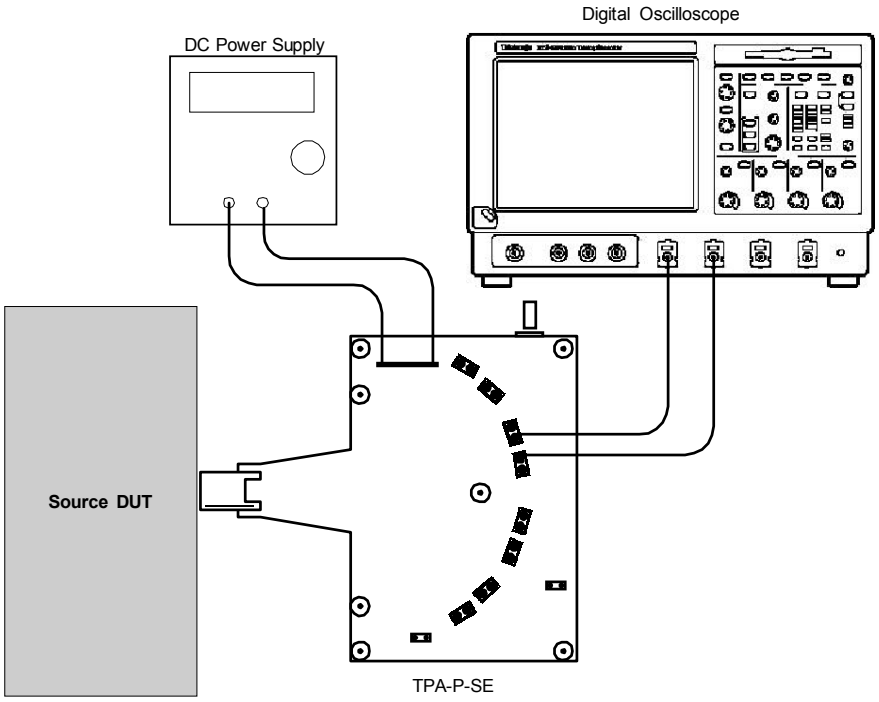
Test Objective

Confirm that any skew within any one differential pair in the TMDS portion of the HDMI link does not exceed the limits in the specification.

Required Test Method

- Connect TPA-P adapter to the Source DUT HDMI output connector.
- Connect first single-ended probe to TMDS_DATA0+.
- Connect second single-ended probe to TMDS_DATA0-.
- Configure Source DUT to output a video format with highest supported pixel clock frequency.
- Measure skew between + and – signals.
- If (skew > $0.15*T_{BIT}$) → FAIL.
- Repeat the test for all remaining TMDS differential pairs.

Recommended Test Method Test ID 7-7: TMDS – Intra-Pair Skew



Setup 12. Test ID 7-7: TMDS – Intra-Pair Skew

No.	Description	Recommended TE	Reference	Qty.
1	4GHz Digital Oscilloscope	Tektronix TDS7404	4.2.1.3	1
2	Single-Ended Probes	Tektronix P7240	4.2.1.5	2
3	DC Power Supply 3.3V	KENWOOD PW18-1.8AQ	4.2.1.14	1
4	EDID Emulator	Silicon Image TE9100	4.2.3.2	1
5	TPA-P-SE Fixture	Tektronix TPA-P-SE	4.2.1.1.4	1

- Connect TPA-P-SE adapter to the Source DUT HDMI output connector.
- Connect first single-ended probe to TMDS_DATA0+.
- Connect second single-ended probe to TMDS_DATA0-.
- Configure Source DUT to output a video format with highest supported pixel clock frequency.
- Set the trigger on TMDS_DATA0+ rising edge.
- Display the waveform of TMDS_DATA0+ and DATA0-. Accumulate at least 10,000 triggers, and determine the most common TMDS_DATA0- 50% point using a Histogram method.
- Measure skew from trigger point to 50% point of first edge of TMDS_DATA0-.
- If (skew > $0.15*T_{BIT}$) → FAIL.
- Repeat the test for all remaining TMDS differential pairs.

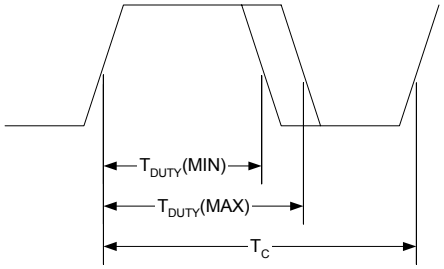
Test ID 7-8: TMDS – Clock Duty Cycle

Reference	Requirement
[HDMI: 4.2.4] HDMI Source TMDS Characteristics	"The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11."
[HDMI: Table 4-13] Source AC Characteristics at TP1	Clock duty cycle must be at least 40% and not more than 60%.

Test Objective

Confirm that the duty cycle of the differential TMDS clock does not exceed the limits allowed by the specification.

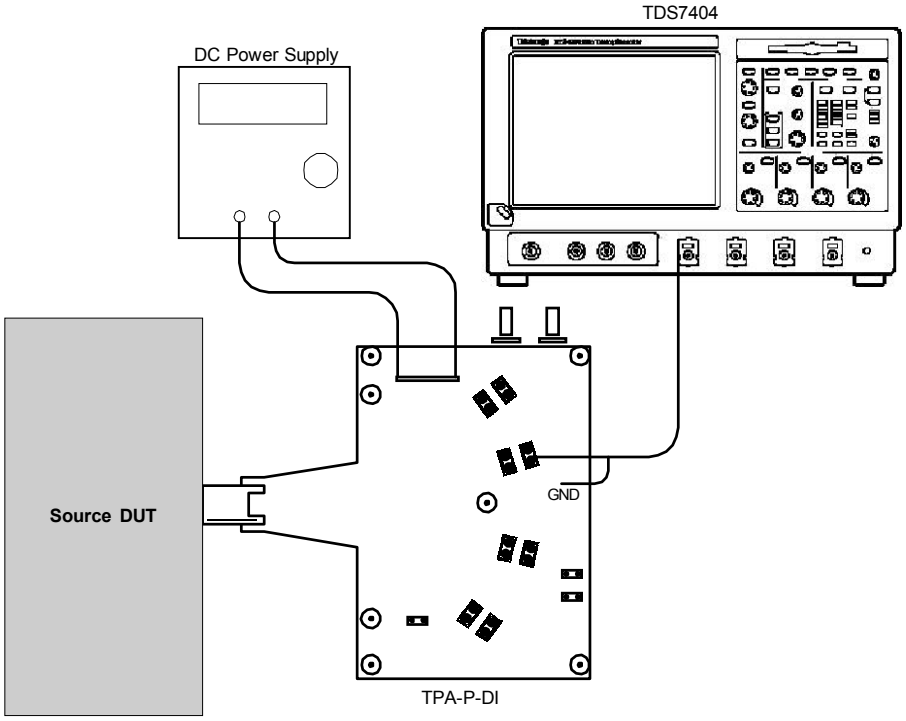
Required Test Method



TMDS AC Clock Duty

- Connect TPA-P adapter to Source DUT HDMI output connector.
- Configure Source DUT to output a video format with highest supported pixel clock frequency.
- Connect differential probe to TMDS Clock.
- Measure minimum duty cycle
- Measure maximum duty cycle
- If (T_{DUTY}(MIN) < 40%) OR (T_{DUTY}(MAX) > 60%) then FAIL.

Recommended Test Method Test ID 7-8: TMDS – Clock Duty Cycle



Setup 13. Test ID 7-8: TMDS – Clock Duty Cycle

No.	Description	Recommended TE	Reference	Qty.
1	4GHz Digital Oscilloscope	Tektronix TDS7404	4.2.1.3	1
2	Differential Probe	Tektronix P7330	4.2.1.4	1
3	DC Power Supply 3.3V	KENWOOD PW18-1.8AQ	4.2.1.14	1
4	EDID Emulator	Silicon Image TE9100	4.2.3.2	1
5	TPA-P-DI Fixture	Tektronix TPA-P-DI	4.2.1.1.2	1

- Connect TPA-P-DI adapter to Source DUT HDMI output connector.
- Configure Source DUT to output a video format with highest supported pixel clock frequency.
- Connect differential probe to TMDS Clock.
- Display the waveform of 1 clock period.
- Configure the oscilloscope: trigger source is the TMDS Clock rising edge, turn on infinite persistence, measurement is duty cycle, capture at least 10,000 triggers.
- Measure minimum duty cycle as earliest crossing of TMDS_CLOCK falling edge.
- Measure maximum duty cycle as latest crossing of TMDS_CLOCK falling edge.
- If (T_{DUTY}(MIN) < 40%) OR (T_{DUTY}(MAX) > 60%) then FAIL.

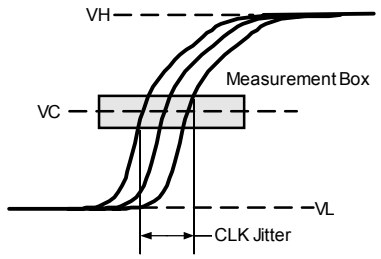
Test ID 7-9: TMDS – Clock Jitter

Reference	Requirement
[HDMI: 4.2.4] HDMI Source TMDS Characteristics	"The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11."
[HDMI: Table 4-13] Source AC Characteristics at TP1	TMDS differential clock jitter must not exceed 0.25*T_{BIT}, relative to the ideal Recovery Clock.

Test Objective

Confirm that the TMDS Clock does not carry excessive jitter.

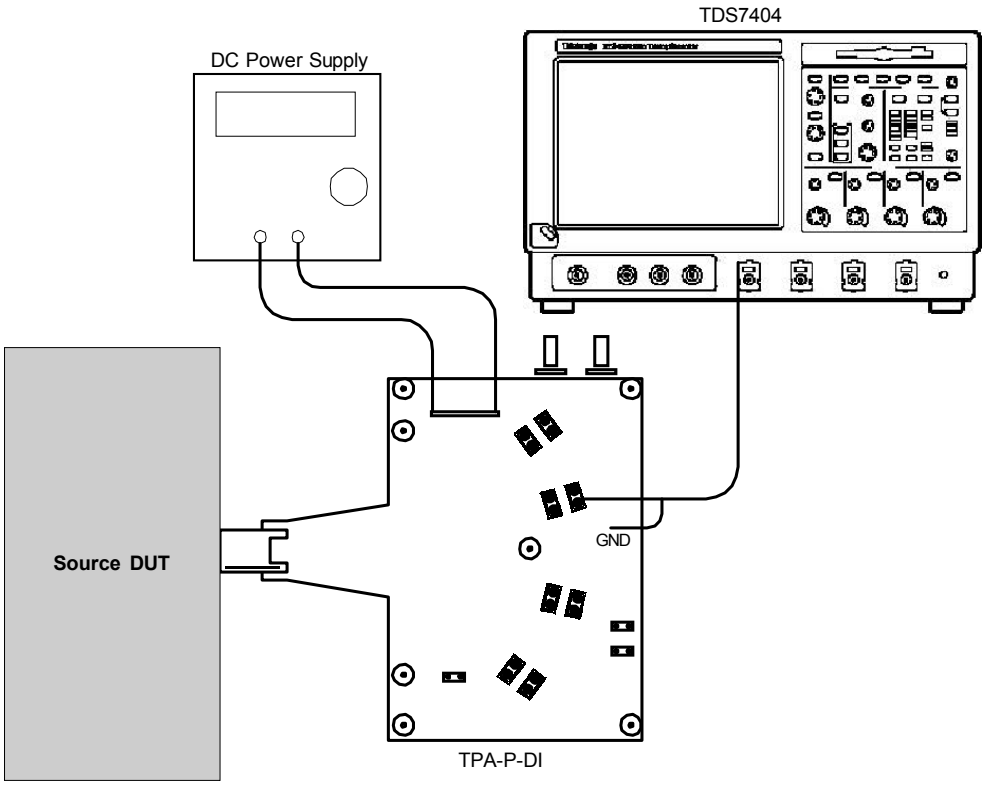
Required Test Method



TMDS AC Clock Jitter

- Connect TPA-P adapter to the Source DUT HDMI output connector.
- Configure Source DUT to output a video format with highest supported pixel clock frequency.
- Connect differential probe to TMDS Clock.
- Configure oscilloscope and Software CRU:
- Capture the waveform and process it with the Software CRU Jitter/Eye Analyzer
- Measure Clock jitter as difference between farthest left sampling point and farthest right sampling point, within the measurement box below:
  - Center voltage, $V_C = (V_H + V_L) / 2$
  - Vertical setting = V_C ± 20mV.
- If Clock jitter exceeds 0.25* T_{BIT} → FAIL

Recommended Test Method Test ID 7-9: TMDS – Clock Jitter



Setup 14. Test ID 7-9: TMDS – Clock Jitter

No.	Description	Recommended TE	Reference	Qty.
1	4GHz Digital Oscilloscope	Tektronix TDS7404	4.2.1.3	1
2	Differential Probe	Tektronix P7330	4.2.1.4	1
3	DC Power Supply 3.3V	KENWOOD PW18-1.8AQ	4.2.1.14	1
4	Software CRU	Tektronix SoftCRU	4.2.1.2	1
5	EDID Emulator	Silicon Image TE9100	4.2.3.2	1
6	TPA-P-DI Fixture	Tektronix TPA-P-DI	4.2.1.1.2	1

- Connect TPA-P-DI adapter to the Source DUT HDMI output connector.
- Configure Source DUT to output a video format with highest supported pixel clock frequency.
- Connect differential probe to TMDS Clock.
- Configure oscilloscope:
  - Single-shot trigger by rising edge of TMDS Clock.
  - Memory length of at least 16M words.
  - Sampling rate of at least 10GHz.
- Configure Software CRU:

  - Software CRU input is TMDS Clock.
  - Software CRU setting is $H(s) = 1 / (1+s\tau)$, where τ = 40nsec.
  - Drawing window size: horizontal is $\pm 1.0 * T_{PIXEL}$.
- Capture the waveform on the oscilloscope.
- Transfer the data capture file to the PC containing the Software CRU. Run the Software CRU.
- Draw TMDS waveform with positive edge trigger generated by Software CRU.
- Measure Clock jitter as difference between farthest left sampling point and farthest right sampling point, within the measurement box below:
  - Center voltage, $V_C = (V_H + V_L) / 2$
  - Vertical setting = $V_C \pm 20$mV.
- If Clock jitter exceeds $0.25 * T_{BIT}$ → FAIL

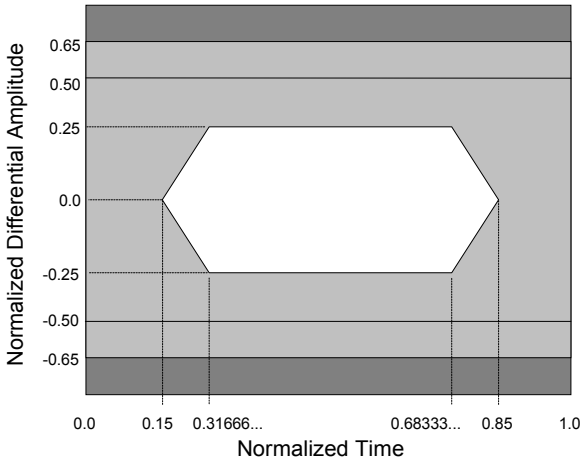
Test ID 7-10: TMDS – Data Eye Diagram

Reference	Requirement
[HDMI: 4.2.4] HDMI Source TMDS Characteristics	"For all channels under all operating conditions specified in Table 4-11 … the Source shall have output levels at TP1, which meet the normalized eye diagram requirements of Figure 4-12."
[HDMI: Figure 4-12] Normalized Eye Diagram Mask at TP1	Refer to the [HDMI: Figure 4-12] "Normalized Eye Diagram Mask at TP1 for Source Requirements"

Test Objective

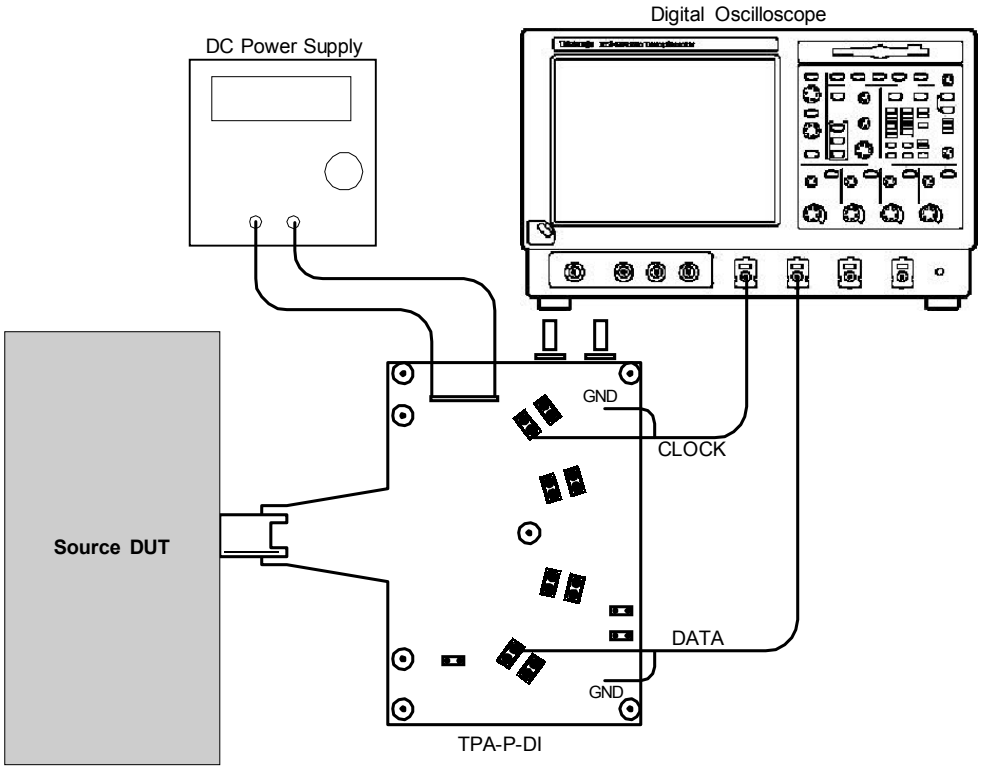
Confirm that the differential signal on each TMDS differential data pair has an "eye opening" (region of valid data) which meets or exceeds the limits on eye opening in the specification.

Required Test Method



- Connect TPA-P to Source DUT HDMI output connector.
- Connect probes to TMDS Clock and TMDS_DATA0
- Configure Source DUT to output first supported video format.
- Configure oscilloscope and Software CRU:
- Capture the waveforms and process it with the Software CRU Jitter/Eye Analyzer
- Compare the data eye to the TP1 Eye Diagram Mask:
  - Shift the mask left until one of the left-side corners touches the waveform.
  - If any other part of the waveform touches or crosses into the data eye, then FAIL.
- Repeat the test for all remaining TMDS_DATA pairs.
- Repeat the test for all supported pixel clock rates. Only one video format is required per pixel clock rate.

Recommended Test Method Test ID 7-10: TMDS – Data Eye Diagram



Setup 15. Test ID 7-10: TMDS – Data Eye Diagram

No.	Description	Recommended TE	Reference	Qty.
1	4GHz Digital Oscilloscope	Tektronix TDS7404	4.2.1.3	1
2	Differential Probe	Tektronix P7330	4.2.1.4	2
3	Software CRU	Tektronix SoftCRU	4.2.1.2	1
4	DC Power Supply 3.3V	KENWOOD PW18-1.8AQ	4.2.1.14	1
5	EDID Emulator	Silicon Image TE9100	4.2.3.2	1
6	TPA-P-DI Fixture	Tektronix TPA-P-DI	4.2.1.1.2	1

- Connect TPA-P-DI to Source DUT HDMI output connector.
- Connect differential probe to TMDS Clock, and configure as trigger.
- Connect second differential probe to TMDS_DATA0.
- Configure Source DUT to output first supported video format.
- Configure the oscilloscope:
  - Memory length of at least 16M points.
  - Single-shot trigger at rising edge of TMDS Clock.

- Sampling rate of at least 10GHz.

- Capture the waveforms on the oscilloscope.
- Transfer the data capture files to the PC containing the Software CRU. Run the Software CRU.
- Configure Software CRU:
  - Software CRU input is TMDS CLOCK and TMDS_DATA0.
  - Software CRU setting is $H(s) = 1 / (1+s\tau)$, where τ = 40nsec.
  - Drawing window size: horizontal is $\pm 1.0 * T_{PIXEL}$.
- Draw TMDS waveform with positive edge trigger generated by the Software CRU.
- Compare the data eye to the TP1 Eye Diagram Mask:
  - Shift the mask left until one of the left-side corners touches the waveform.
  - If any other part of the waveform touches or crosses into the data eye, → FAIL.
- If data jitter > $0.3 * T_{BIT}$ → FAIL.
  - Measurement box vertical setting : Vcenter = (VH + VL) / 2 = ±5mV
- Repeat the test for all remaining TMDS_DATA pairs.
- Repeat the test for all supported pixel clock rates. Only one video format is required per pixel clock rate.

Test ID 7-11: +5V Power

Reference	Requirement
[HDMI: 4.2.7] +5V Power Signal	"All Sources shall assert the +5V Power signal whenever the source is using the DDC, CEC or TMDS signals."
[HDMI: Table 4-19] Power Pin Voltage	Power pin voltage shall be 4.95V to 5.05V at TP1. [Note: An errata changing this range to 4.9V to 5.1V will be issued.]

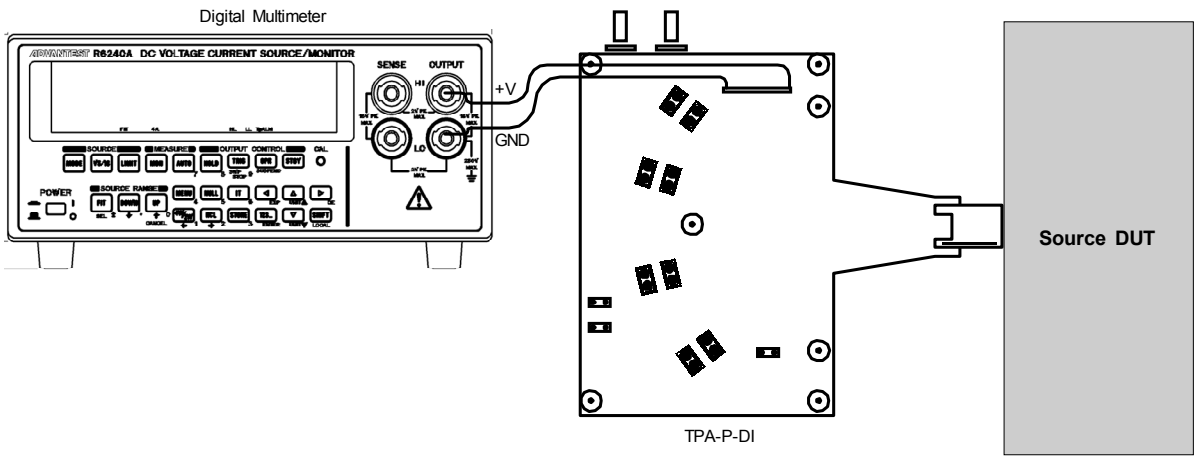
Test Objective

Confirm that +5V Power signal meets voltage and current capacity requirements.

Required Test Method

- Connect TPA-P adapter to Source DUT HDMI output connector.
- While drawing 55mA from the +5V Power pin, measure the voltage, V_{5V}.
- If (V_{5V} < 4.9V) OR (V_{5V} > 5.1V) then FAIL
- Repeat the test after setting up the multi-meter to draw 0mA from the pin.

Recommended Test Method Test ID 7-11: +5V Power



Setup 16. Test ID 7-11: +5V Power

No.	Description	Recommended TE	Reference	Qty.
1	Digital Multi-Meter	ADVANTEST R6240A	4.2.1.11	1
2	EDID Emulator	Silicon Image TE9100	4.2.3.2	1
3	TPA-P-DI Fixture	Tektronix TPA-P-DI	4.2.1.1.2	1

- Connect TPA-P-DI adapter to Source DUT HDMI output connector.
- Connect the R6240A ISVM-type Multi-meter to the +5V Power signal on the TPA fixture..
- Setup the Multi-Meter to draw 55mA from the pin, while measuring the voltage, V_{5V}.
- If (V_{5V} < 4.9V) OR (V_{5V} > 5.1V) then FAIL
- Repeat the test after setting up the multi-meter to draw 0mA from the pin.

Test ID 7-12: Hot Plug Detect

Reference	Requirement
[HDMI: Table 4-22] Required Output Characteristics of Hot Plug Detect Signal	High voltage level (Sink) Minimum 2.4 Volts, Maximum 5.05 Volts Low voltage level (Sink) Minimum 0 Volts, Maximum 0.4 Volts Output resistance 1000 ohms ±20%
[HDMI: Table 4-23] Required Detect Levels for Hot Plug Detect Signal	The high voltage level must be within 2.0V to 5.05V. The low voltage level must be within 0.0V to 0.8V. [Note: An errata changing the maximum high voltage level to 5.1V will be issued.]

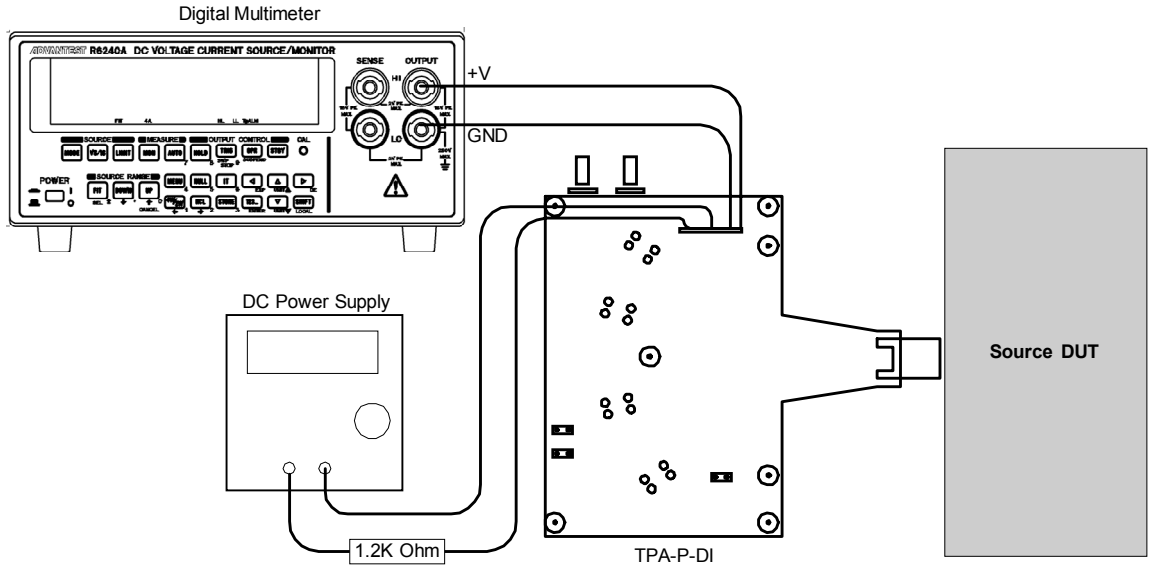
Test Objective

Confirm that the Source load on the Hot Plug pin allows the signal to meet the specified requirements.

Required Test Method

- Connect power supply (+) to HPD through a 1.2KΩ resistor and (-) to ground.
- For each of the following tests, measure the voltage, V_{HPD}, at the input point of the Source's HPD pin.
- Apply DC power of 2.4V and 5.1V. For each:
  - Measure the voltage level at the HPD input: V_{HPD}(HIGH).
  - If (V_{HPD}(HIGH) < 2.0V) OR (V_{HPD}(HIGH) > 5.1V) then FAIL.
- Apply DC power of 0.0V and 0.4V. For each:
  - Measure the voltage level at the HPD input: V_{HPD}(LOW).
  - If (V_{HPD}(LOW) < 0.0V) OR (V_{HPD}(LOW) > 0.80V) then FAIL.

Recommended Test Method Test ID 7-12: Hot Plug Detect



Setup 17. Test ID 7-12: Hot Plug Detect

No.	Description	Recommended TE	Reference	Qty.
1	Digital Multi-meter	ADVANTEST R6240A	4.2.1.11	1
2	DC Power Supply	KENWOOD PW18-1.8AQ	4.2.1.14	1
3	1.2KΩ ± 1% resistor	<Any>		1
4	EDID Emulator	Silicon Image TE9100	4.2.3.2	1
5	TPA-P-DI Fixture	Tektronix TPA-P-DI	4.2.1.1.2	1

- Connect power supply (+) to HPD through a 1.2KΩ resistorand (–) to ground.
- For each of the following tests, measure the voltage, V_{HPD}, at the input point of the Source's HPD pin.
- Apply DC power of 2.4V and 5.1V. For each:
  - Measure the voltage level at the HPD input: V_{HPD}(HIGH).
  - If (V_{HPD}(HIGH) < 2.0V) OR (V_{HPD}(HIGH) > 5.1V) then FAIL.
- Apply DC power of 0.0V and 0.4V. For each:
  - Measure the voltage level at the HPD input: V_{HPD}(LOW).
  - If (V_{HPD}(LOW) < 0.0V) OR (V_{HPD}(LOW) > 0.80V) then FAIL.

Test ID 7-13: DDC/CEC Capacitance

Reference	Requirement
[HDMI: 4.2.8] DDC	"The Display Data Channel (DDC) I/Os and wires … shall meet the requirements specified in the I^2C Specification, version 2.1, Section 15 for 'Standard Mode' devices."
[HDMI: Table 4-20] Maximum Capacitance of DDC Line	SDA capacitance must be ≤ 50pF at the Source. SCL capacitance must be ≤ 50pF at the Source.
[HDMI: Table 4-24] CEC line Electrical Specifications for all Configurations	Maximum capacitance load of a device (excluding cable) 100pF CEC Line Capacitance

Test Objective

Confirm that the capacitance load on the DDC and CEC lines does not exceed the limit in the specification.

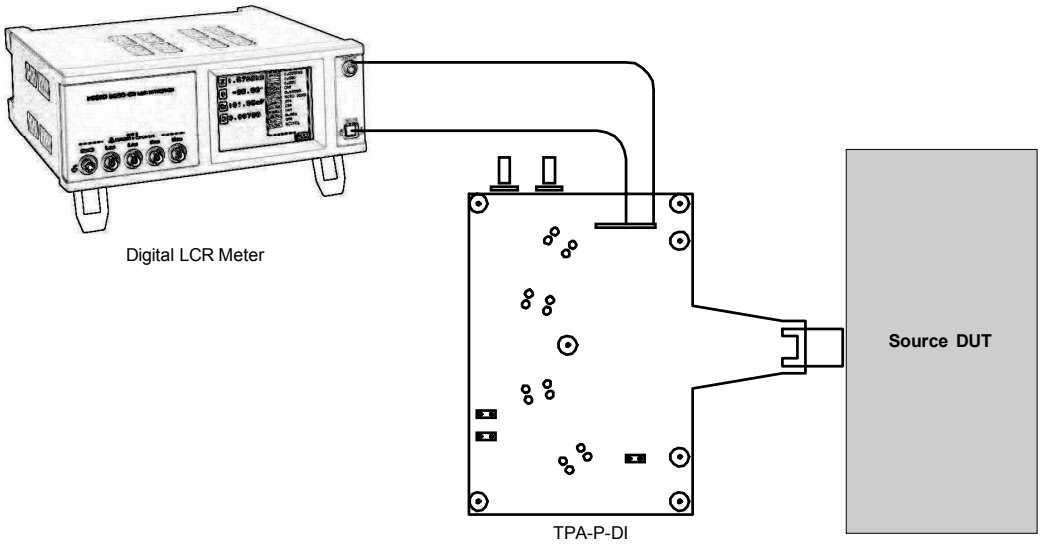
Required Test Method

- Turn off power to the Source DUT.
- Set the LCR meter test signal:
  - Frequency = 100kHz
- Measure C1 as the inherent TPA-P-DI capacitance on the SDA pin.
- Attach TPA-P-DI to Source DUT and measure capacitance C2 on SDA.
- Net Source DUT capacitance, C_{SOURCE} = C2 – C1.
- If C_{SOURCE} > 50pF, then FAIL.

- Repeat the C1 and C2 measurement for the SCL pin.
- If C_{SOURCE} > 50pF, then FAIL.

- Set the LCR meter test signal:
  - Frequency = 1kHz
- Repeat the C1 and C2 measurement for the CEC pin.
- If C_{SOURCE} > 100pF, then FAIL.

Recommended Test Method Test ID 7-13: DDC/CEC Capacitance



Setup 18. Test ID 7-13: DDC/CEC Capacitance

No.	Description	Recommended TE	Reference	Qty.
1	Digital LCR Meter	HIOKI 3522-50	4.2.1.15	1
2	LCR Meter Probe	HIOKI 9143	4.2.1.15	1
3	TPA-P-DI Fixture	Tektronix TPA-P-DI	4.2.1.1.2	1

- Turn off power to the Source DUT.
- Calibrate the capacitance probe.
- Set LCR meter test signal:
  - DC Bias voltage = 2.5V
  - AC voltage = 2.5V peak-to-peak
  - Frequency = 100kHz
- Measure C1 as the inherent TPA-P-DI capacitance on the SDA pin.
- Attach TPA-P-DI to Source DUT and measure capacitance C2 on SDA.
- Net Source DUT capacitance, C_{SOURCE} = C2 – C1.
- If C_{SOURCE} > 50pF, then FAIL.
- Repeat the C1 and C2 measurement for the SCL pin.
- If C_{SOURCE} > 50pF, then FAIL.
- Set the LCR meter test signal:
  - Frequency = 1kHz
- Repeat the C1 and C2 measurement for the CEC pin.
- If C_{SOURCE} > 100pF, then FAIL.

Test ID 7-14: CEC Line Connectivity

NOTE: This test only needs to be performed once per product, not once per connector as with all of the other tests in this document.

Reference	Requirement
[HDMI: Table 4-24] CEC Line Connectivity	<See reference for details>

Test Objective

If the DUT has more than one input connection ensure that any input connections and output connections are connect as specified in following description:

CEC lines from all HDMI inputs (if present) and a single HDMI output (if present) shall be interconnected.

Except :

- A device which has no HDMI output is allowed to have separate CEC lines for each HDMI connector if that device takes a logical address of 0 on each CEC line.
- A TV that is acting as the root shall not connect the CEC line to any HDMI output.

Required Test Procedure

- Turn DUT off
- If CDF field CDF_HDMI_output_count == 0 then:
  - For every combination of HDMI connectors on the DUT measure the resistance between the CEC connection of each. If each resistance measurement is less than 2Ω or greater than 48KΩ then PASS else FAIL.
- else
  - If CDF field Sink_Display == Y then:
    - For every combination of HDMI input connectors on the DUT measure the resistance between the CEC connections of each. If any resistance measurement is in range 2Ω < R < 48KΩ then FAIL
    - For every output connection measure the resistance between its CEC connections of it and each input connection. If any resistance measurement is in less than 1MΩ then FAIL else PASS.
  - Else:
    - For every combination of HDMI input connectors on the DUT measure the resistance between the CEC connections of each. If any resistance measurement > 2Ω then FAIL
    - For every output connection measure the resistance between the CEC connections of it and each input connection. If any resistance measurement is in less than 1MΩ then note the output connection ID.

- If more than one output connection ID noted then FAIL (as product has CEC line connected to > 1 output)
- Choose any input connector on the DUT measure the resistance between the CEC connection of this input and the CEC connection of the noted output connection. If resistance measurement > 2Ω then FAIL else PASS.

Recommended Test Method

No.	Description	Recommended TE	Reference	Qty.
1	Digital Multi-Meter	ADVANTEST R6240A	4.2.1.11	1
2	TPA-P-SE	Tektronix TPA-P-SE	4.2.1.1.4	1
3	TPA-P-DI	Tektronix TPA-P-DI	4.2.1.1.2	1

- Turn DUT off
- Set Digital Multi-Meter to measure resistance using auto scale mode.
- If CDF field CDF_HDMI_output_count == 0:
  - For every combination of HDMI connectors on the DUT
    - Connect TPA-P to each selected HDMI connector
    - Connect the meter to the CEC connection on each TPA-P
    - Read resistance value from Digital Multi-Meter
    - If reading is less than 2Ω or greater than 48KΩ → PASS, else FAIL
- else:
  - If CDF field Sink_Display == Y then:
    - For every combination of HDMI input connectors on the DUT
      - Connect TPA-P to each selected HDMI connector
      - Connect the meter to the CEC connection on each TPA-P
      - Read resistance value from Digital Multi-Meter
      - If reading is less than 2Ω or greater than 48KΩ → PASS and continue else FAIL
    - For every output connection:
      - Connect TPA-P to each selected HDMI connector
      - Connect the meter to the CEC connection on each TPA-P
      - Read resistance value from Digital Multi-Meter
      - If reading is less than 48KΩ → FAIL
  - Else (CDF field Sink_Display == N)
    - For every combination of HDMI input connectors on the DUT
      - Connect TPA-P to each selected HDMI connector
      - Connect the meter to the CEC connection on each TPA-P

- Read resistance value from Digital Multi-Meter
- If reading is greater than 2Ω → FAIL

- For every output connection:
  - Connect TPA-P to each selected HDMI connector
  - Connect the meter to the CEC connection on each TPA-P
  - Read resistance value from Digital Multi-Meter
  - If reading is less than 48KΩ then note the output connection ID
- If more than one output connection ID noted → FAIL (as product has CEC line connected to > 1 output)
- If no output connection ID noted → FAIL (as product does not connect CEC line to any output)
- Choose any input connector on the DUT connect TPA-P to it,connect the Digital Multi-Meter to its CEC connection
- Connect TPA-P to noted output connection and Digital Multi-Meter Probe to its CEC connection
- Read resistance value from Digital Multi-Meter
- If reading is >2Ω → FAIL else PASS

Test ID 7-15: CEC Line Degradation

NOTE: This test only needs to be performed once per product, not once per connector as with all of the other tests in this document.

Reference	Requirement
[HDMI: Table 4-24] Power off characteristics	<See reference for details>

Test Objective

Ensure that the DUT does not degrade communication between other CEC devices when power is applied, when power is removed and, if supported, in standby mode (the line must not be pulled down by the powered off device).

Required Test Procedure

- Measure CEC line voltage on DUT, V_{CEC1}, if voltage 0v or 3.3v ±10% then continue else → FAIL
- Connect the CEC line on DUT to 3.3v via a 27Kohm ±5% resistor
- Measure CEC line voltage if voltage not 3.3v ±10% then → FAIL
- Connect the CEC line on the DUT input connector to DDC/CEC Ground via 1k ohm ±5% load resistor (as well as the previously connected 3.3v via 27KΩ)
- Measure CEC line voltage on the DUT output connector, V_{CEC2}
- If V_{CEC1} = 0v and V_{CEC2} not in range 0.12v ±12% then → FAIL
- If V_{CEC1} = 3.3v ±10% and V_{CEC2} not 0.24v ±12% then → FAIL
- Repeat tests in power off state
- If standby power mode exists on DUT, repeat test in that state

Recommended Test Method

No.	Description	Recommended TE	Reference	Qty.
1	Digital Multi-Meter	ADVANTEST R6240A	4.2.1.11	1
3	27KΩ ±5% resistor	<any>		1
3	1KΩ±5% Resistor	<any>		1
4	TPA-P-SE	Tektronix TPA-P-SE	4.2.1.1.4	1

- Power on DUT
- Connect TPA to DUT
- Set DC Power Supply to 3.3V
- Set Multi-Meter to voltage measurement and connect between CEC pin and DDC/CEC Ground on TPA

- Measure voltage with multi-Meter, record as V_{CEC1}
- if V_{CEC1} 0v or 3.3v ±10% then continue else → FAIL
- Connect the CEC line on TPA to DC Power Supply via the 27Kohm ±5% resistor
- Measure voltage if voltage not 3.3v ±10% then → FAIL
- Connect the CEC line on the TPA input connector to DDC/CEC Ground on TPA via 1k ohm ±5% load resistor (as well as the previously connected 3.3v via 27KΩ)
- Measure voltage, record as V_{CEC2}
- If V_{CEC1} = 0v and V_{CEC2} not in range 0.12v ±12% then → FAIL
- If V_{CEC1} = 3.3v ±10% and V_{CEC2} not 0.24v ±12% then → FAIL
- Repeat tests in power off state
- If standby power mode exists on DUT, repeat test in that state

7.4 Source – Protocol

7.4.1 Required Test Method Setup for Protocol Tests

Unless stated otherwise, the Required Test Method for all of the tests in Section 7.4 includes the following setup and Source DUT operation:

- Connect Source DUT to an Encoding Analyzer or Protocol Analyzer as specified in test.
- Operate the Source DUT to transmit any one of the following video format timings for at least 2 seconds while also transmitting 2-channel PCM audio (if supported) at the highest supported audio sampling rate:
  - 720x480p @ 59.94Hz
  - 640x480p @ 59.94Hz
  - 720x576p @ 50Hz
- Perform the specified protocol test(s) for an analysis period of at least two seconds.
- Operate the Source DUT to transmit the first of the following video format timings which is supported by the DUT (if any are supported) while also transmitting 2-channel PCM audio (if supported) at the highest supported audio sampling rate:
  - 1080i @ 60Hz
  - 720p @ 60Hz
  - 1080i @ 50Hz
  - 720p @ 50Hz
- Perform the specified protocol test(s) for the entire analysis period.

7.4.2 Tests

Test ID 7-16: Legal Codes

Reference	Requirement
[HDMI: 5.1.2] Operating Modes Overview	"The HDMI link operates in one of three modes: Video Data Period, Data Island period, and Control period."
[HDMI: 5.2.2.1] Video Guard Band	<See reference for details.>
[HDMI: 5.2.3.3] Data Island Guard Band	<See reference for details.>
[HDMI: 5.4.2] Control Period Coding	<See reference for details.>
[HDMI: 5.4.3] TERC4 Coding	<See reference for details.>
[HDMI: 5.4.4] Video Data Coding	<See reference for details.>

Test Objective

Verify that Source only outputs legal 10-bit codes.

Required Test Method

Connect DUT to a recommended Encoding Analyzer and operate Source DUT as described in Section 7.4.1.

- Verify that, for all pixels within the analysis period, the Source DUT transmits only 10-bit values on each of the three TMDS channels that correspond to one of the following:
  - Any legal Video Data codes
    - Any Video Data Code that was encoded with an incorrect "data stream disparity" value, that is, which causes the channel to become more, rather than less DC-balanced.
  - 4 Control Period codes
  - 16 TERC4 codes
  - Data Island Guard Band (all 4 possible values for Channel 0)
  - Video Guard Band
- [Illegal 10-bit code] If any channel contains a 10-bit code that is not one of the above → FAIL
- Verify that, for all pixels, all three TMDS channels are encoded using the same of the 5 encodings above.
- [Inconsistent channel coding] If any pixel does not use consistent encoding across all three channels → FAIL

Recommended Test Method Test ID 7-16: Legal Codes

Setup Source DUT and P/A/V Analyzer and operate Source DUT as described in Section 7.4.1.

- HDMI Analysis command: ’Full HDMI Compliance‘ or ’Illegal Codes’
- If HDMI Analysis reports ‘PASS’, then PASS, else FAIL

Test ID 7-17: Basic Protocol

Reference	Requirement
[HDMI: 5.2.1.1] Preamble	"Immediately preceding each Video Data Period or Data Island Period is the Preamble. This is a sequence of eight identical Control characters that indicate whether the upcoming data period is a Video Data Period or is a Data Island."
[HDMI: 5.2.2] Video Data Period	"…the Video Data Period begins with a two pixel Video Leading Guard Band."
[HDMI: 5.2.3] Data Island Period	"The first two data characters within the Data Island are the Leading Guard Band. The last two data characters within the Data Island are the Trailing Guard Band."
[HDMI: Table 5-3] TMDS Link Timing Parameters	"Minimum duration Control Period: 12 T_{PIXEL}"
[HDMI: 5.4] Encoding	<See reference for details.>

Test Objective

Verify that Source only outputs code sequences for Control Periods, Data Island Periods and Video Data Periods corresponding to basic HDMI protocol rules.

Required Test Method

Connect Source DUT to a Protocol Analyzer and operate as described in Section 7.4.1.

- For every transition from a pixel with Control Period Coding to next pixel using any other (non-Control) encoding:
  - If the 12 pixels prior to the transition contain any pixels not encoded with Control Period Coding → FAIL, (Control Period too short)
  - Examine the CTL3:CTL2:CTL1:CTL0 values for the 8 (Control-encoded) pixels prior to the transition and compare to the values 0b0001 (Video Data Period Preamble) and 0b0101 (Data Island Preamble).
  - [Inconsistent Preamble]
  - If any of the 8 pixels does not match the CTLx value for any of the other 7 pixels → FAIL
  - [Illegal Preamble]
  - If the Preamble value is neither Data Island Preamble nor Video Data Preamble → FAIL
  - If the Preamble value is Data Island Preamble:
    - Examine the first two pixels following the Preamble (Leading Guard Band).
    - If either of these pixels does not equal one of the 4 permitted Data Island Guard Band characters [HDMI: 5.2.3.3] → FAIL
    - Scan through following pixels, while counting pixels, until finding a transition to Control Period Coding, verifying that every pixel is encoded with Data Island Coding.

- Examine the last two pixels preceding this transition (Trailing Guard Band).
- If either of these pixels does not equal one of the 4 permitted Data Island Guard Band characters [HDMI: 5.2.3.3] → FAIL
- If any pixel following the Leading Guard Band but preceding the Trailing Guard Band is not a legal TERC4 code → FAIL
- If first pixel following the Leading Guard Band has TERC4 ch. 0, bit 3 = 1 → FAIL
- If any other pixel prior to Trailing Guard Band has TERC4 ch. 0, bit 3 == 1 → FAIL
- Length of Data Island is equal to number of pixels following Leading Guard Band and prior to Trailing Guard Band. Number of packets = Length of Data Island / 32.
- If number of packets is not an integer → FAIL
- If number of packets == 0 → FAIL
- If number of packets > 18 → FAIL
- For every packet within the Data Island:
  - For each of the 5 ECC blocks within the packet:
    - If BCH parity bits are incorrect → FAIL

- If the Preamble value is Video Data Preamble:
  - Examine the first two pixels following the Preamble.
  - If either of these pixels does not equal the Video Data Guard Band character [HDMI: 5.2.2.1] → FAIL
  - Scan through following pixels until finding a transition to Control Period Coding, verifying that every pixel is encoded with Video Data Coding.
  - If any pixel following Video Guard Band up to transition is not a correctly encoded Video Data code → FAIL
- If no “FAIL” above, then → PASS

Recommended Test Method — Test ID 7-17: Basic Protocol

Setup Source DUT and P/A/V Analyzer and operate Source DUT as described in Section 7.4.1.

- HDMI Analysis command: ’Full HDMI Compliance‘ or ’Basic Protocol’
- If HDMI Analysis reports ‘PASS’, then PASS, else FAIL

Test ID 7-18: Extended Control Period

Reference	Requirement
[HDMI: Table 5-4] Extended Control Period Parameters	Maximum time between Extended Control Periods 50 msec Minimum duration Extended Control Period 32 T_{PIXEL}

Test Objective

Verify that Source outputs an Extended Control Period within the required period.

Required Test Method

Connect Source DUT to a Protocol Analyzer and operate as described in Section 7.4.1.

- Starting with the first pixel of the capture, perform the following search for each 50milliseconds of capture
  - [Search for Extended Control Period]
  - If no Control Period within the 50msecs is 32 or more pixels in length → FAIL
  - If any Control Period within the 50msecs is 32 or more pixels in length → CONTINUE

Recommended Test Method

Setup Source DUT and P/A/V Analyzer and operate Source DUT as described in Section 7.4.1.

- HDMI Analysis command: 'Full HDMI Compliance' or 'Extended Control Period'
- If HDMI Analysis reports 'PASS', then PASS, else FAIL

Test ID 7-19: Packet Types

Reference	Requirement
[HDMI: 5.3] Data Island Packets	<See reference for details.>

Test Objective

Verify that Source only transmits permitted Packet Types and that reserved fields are zero.

Required Test Method

Connect Source DUT to a Protocol Analyzer and operate as described in Section 7.4.1.

- If no Data Island is detected at least once per video field → FAIL
- For each Packet within each Data Island in the capture:
  - If packet type is not equal to any of the following: 0x00, 0x01, 0x02, 0x03, 0x81, 0x82, 0x83, 0x84, 0x85 → FAIL, (optionally continue to next packet)
  - If packet type is equal to 0x00 (Null Packet)
    - Check bytes HB1, HB2 and all bytes in packet body.
    - If any bytes do not equal 0x00 → FAIL
  - If packet type is equal to 0x01 (ACR Packet)
    - Check bytes HB1, HB2.
    - If HB1 or HB2 does not equal 0x00 → FAIL
    - Check byte SB0 of subpacket 0
    - If SB0 does not equal 0x00 → FAIL
    - Check byte SB1 of subpacket 0
    - If bits 7, 6, 5 and 4 of SB0 do not equal 0x00 → FAIL
    - Check byte SB4 of subpacket 0
    - If bits 7, 6, 5 and 4 of SB4 do not equal 0x00 → FAIL
    - Compare SB0…SB6 of subpacket 0 with SB0…SB6 of every other subpacket. Likewise compare subpacket 1 with subpacket 2 and 3 and compare subpacket 2 with subpacket 3.
    - If any subpacket differs from any other → FAIL
  - If packet type is equal to 0x02 (Audio Sample Packet)
    - Check byte HB1.
    - If bits 7, 6, and 5 of HB1 do not equal 0 → FAIL
  - If packet type is equal to 0x03 (General Control Packet)
    - Check bytes HB1, HB2.
    - If either byte does not equal 0x00 → FAIL

- Check byte SB0 of subpacket 0.
- If SB0 does not equal 0x00, 0x01, or 0x10 → FAIL
- Check bytes SB1…SB6 of subpacket 0.
- If any SB1…SB6 does not equal 0x00 → FAIL
- Compare SB0…SB6 of subpacket 0 with SB0…SB6 of subpackets 1, 2 and 3. Likewise compare subpacket 1 with subpacket 2 and 3 and compare subpacket 2 with subpacket 3.
- If any subpacket differs from any other → FAIL

Recommended Test Method — Test ID 7-19: Packet Types

Setup Source DUT and P/A/V Analyzer and operate Source DUT as described in Section 7.4.1.

- HDMI Analysis command: 'Full HDMI Compliance' or 'Packet Types'
- If HDMI Analysis reports 'PASS', then PASS, else FAIL

7.5 Source – Video

Test ID 7-20: Type A Connector Usage

Reference	Requirement
[HDMI: 4.1.2.1] Connector Support Requirements, HDMI Sources	"An HDMI Source connection using a Type A connector shall transmit only video format timings that are: • Described in Section [HDMI] 6.3, or, • Defined, per EDID Ver. 1.3, in the first, and only the first 18-byte timing descriptor of a concurrently attached HDMI compliant Sink. An HDMI Source connection using a Type B connector may transmit any video format timing."

Test Objective

Verify that Source use of a Type A connector is permitted under rules given above.

Required Test Method

- If Source DUT uses a Type B connector (on the tested port) → PASS
- If CDF field Source_Non-861B_Formats contains "N" → PASS
- If CDF field Source_Established-Timings contains any value other than "N" → FAIL
- If CDF field Source_Standard-Timings contains any value other than "N" → FAIL
- If CDF field Source_DTD_2_end contains any value other than "N" → FAIL

Recommended Test Method

Perform steps in Required Test Method.

Test ID 7-21: Minimum Format Support

Reference	Requirement
[HDMI: 6.2.1] Format Support Requirements	An HDMI Source shall support at least one of the following video format timings: 640x480p @ 59.94/60Hz 720x480p @ 59.94/60Hz 720x576p @ 50Hz

Test Objective

Verify that Source meets minimum Video Format support requirement.

Required Test Method

Check CDF field

Field Name	*Field Definition*	*Choices*	*Repeater Mini-CDF*
Source_861B_Formats	Which EIA/CEA-861B video formats are supported by product?	861B format numbers (1…34)	2 (if 60Hz product) 17 (if 50Hz product)

- for any of the following video format timings.
  - 640x480p @ 59.94/60Hz 4:3 (Format 1)
  - 720x480p @ 59.94/60Hz 4:3 (Format 2) or 16:9 (Format 3)
  - 720x576p @ 50Hz 4:3 (Format 17) or 16:9 (Format 18)
- If CDF contains any of the video format timings → PASS
- Else, FAIL

Recommended Test Method

Perform steps in Required Test Method.

Test ID 7-22: Additional Format Support

Reference	Requirement
[HDMI: 6.2.1] Format Support Requirements	"An HDMI Source that is capable of transmitting any of the following video format timings using any other component analog or uncompressed digital video output, shall be capable of transmitting that video format timing across the HDMI interface. 1280x720p @ 59.94/60Hz 1920x1080i @ 59.94/60Hz 720x480p @ 59.94/60Hz 1280x720p @ 50Hz 1920x1080i @ 50Hz 720x576p @ 50Hz"

Test Objective

Verify that Source is capable of transmitting formats required due to similar support on non-HDMI interfaces.

Required Test Method

- For each of the rows in table below, If CDF field in column "If CDF field…is 'Y'" then:
  - Check CDF field

Field Name	***Field Definition***	***Choices***	***Repeater Mini-CDF***
Source_861B_Formats	Which EIA/CEA-861B video formats are supported by product?	861B format numbers (1…34)	2 (if 60Hz product) 17 (if 50Hz product)

- for the 861B format number(s) in column “CDF…must contain value below”
- If none of these formats is in CDF field

Field Name	*Field Definition*	*Choices*	*Repeater Mini-CDF*
Source_861B_Formats	Which EIA/CEA-861B video formats are supported by product?	861B format numbers (1…34)	2 (if 60Hz product) 17 (if 50Hz product)

- → FAIL, "Missing <Comment text>"

<table>
<tr><td colspan="2">If CDF field below == 'Y'</td><td colspan="2">CDF
<table><tr><th>Field Name</th><th>Field Definition</th><th>Choices</th><th>Repe Mini-CDF</th></tr><tr><td>Source_861B_Formats</td><td>Which EIA/CEA-861B video formats are supported by product?</td><td>861B format numbers (1…34)</td><td>2 (if 6 produ
17 (if 50Hz produ</td></tr></table>must contain value below:</td></tr>
<tr><td colspan="2"><table><tr><th>Field Name</th><th>Field Definition</th><th>Choices</th><th>Repeater Mini-CDF</th></tr><tr><td>Source_480p60</td><td>Tested Format : 720x480p @ 59.94/60Hz

Is DUT capable of transmitting Tested Format using any other component analog or uncompressed digital video output?</td><td>Y/N</td><td>N</td></tr></table></td><td>2 or 3</td></tr>
<tr><td colspan="2">Source_720p60</td><td>4</td></tr>
<tr><td colspan="2">Source_1080i60</td><td>5</td></tr>
<tr><td colspan="2">Source_576p50</td><td>17 or 18</td></tr>
</table>

Source_720p50	19
Source_1080i50	20

Recommended Test Method

Perform steps in Required Test Method.

Test ID 7-23: Pixel Encoding – RGB to RGB-only Sink

Reference	Requirement
[HDMI: 6.2.3] Pixel Encoding Requirements	"All HDMI Sources shall be capable of supporting RGB 4:4:4 pixel encoding."
[HDMI: 6.2.3] Pixel Encoding Requirements	"An HDMI Source may determine the pixel-encodings that are supported by the Sink through the use of the E-EDID. If the Sink indicates that it supports YC_BC_R-formatted video data and if the Source can deliver YC_BC_R data, then it can enable the transfer of this data across the link."
[861B: Table 8] AVI InfoFrame Data Byte 1	<See reference for details (Y1, Y0 field).>

Test Objective

Verify that the Source DUT always outputs required pixel encoding (RGB) which also correlates with AVI field Y when connected to an RGB-only Sink.

Required Test Method

- Attach Source DUT to Video Picture Analyzer containing any valid HDMI EDID with bits 4 and 5 of byte 3 of the CEA EDID Timing Extension both clear (0).
- Operate Source DUT to output video using material or a pattern which can clearly indicate, on the attached Sink, whether the proper pixel encoding is being used. Attempt, through user menus, buttons, etc. to configure Source DUT to use YC_BC_R pixel encoding on transmitted video.
- Examine video output and any AVI InfoFrame transmitted from Source.
- [Verify that transmitted video uses RGB pixel encoding.]
  - Examine image on Video Picture Analyzer.
  - If image appears to be transmitted with a non-RGB pixel encoding → FAIL
- If CDF field Source_AVI_Supported == 'Y':
  - Verify that an AVI InfoFrame is transmitted on every video field.
  - If any video field occurs with no AVI InfoFrame → FAIL
- [Verify that any transmitted AVI InfoFrame is correct and indicates RGB pixel encoding]
  - If any AVI InfoFrame, field Y1 and Y0 does not indicate RGB encoding → FAIL

Recommended Test Method

Perform Required Test Method using either Recommended Video Picture Analyzers

PASS/FAIL criteria is defined above.

Test ID 7-24: Pixel Encoding– YC_BC_R to YC_BC_R Sink

Reference	Requirement
[HDMI: 6.2.3] Pixel Encoding Requirements	"All HDMI Sources shall support either YC_BC_R 4:2:2 or YC_BC_R 4:4:4 pixel encoding whenever that device is capable of transmitting a color-difference color space across any other component analog or digital video interface."
[HDMI: 6.5] Pixel Encodings	<See reference for details.>
[861B: 6.1] Auxiliary Video Information (AVI) InfoFrame	<See reference for details.>

Test Objective

Verify that the Source DUT always outputs pixel encoding that correlates with AVI field Y when presented with a YC_BC_R-capable Sink and that DUT is capable of supporting YC_BC_R pixel encoding when required.

Required Test Method

- Attach Source DUT to Video Picture Analyzer containing any valid HDMI EDID with bits 4 and 5 of byte 3 of the CEA EDID Timing Extension both set (1).
- Operate Source DUT to output video using material or a pattern which can clearly indicate, on the attached Sink, whether the proper color space is being used. Attempt to cause YC_BC_R pixel encoding to be used by Source DUT.
- If CDF field Source_AVI_Supported == 'Y':
  - Verify that an AVI InfoFrame is transmitted on every video field.
  - If any video field occurs with no AVI InfoFrame → FAIL
- Examine video output and all AVI InfoFrames transmitted from Source.
- If AVI Y1 and Y0 fields do not indicate same pixel encoding as is used in transmitted video → FAIL
- If CDF field Source_HDMI_YC_BC_R is "Y" :
  - If transmitted video uses RGB pixel encoding → FAIL
  - If any transmitted AVI InfoFrame indicates RGB pixel encoding → FAIL
- Else, PASS

Recommended Test Method

Perform Required Test Method using either Recommended Video Picture Analyzers

Test ID 7-25: Video Format Timing

Reference	Requirement
[HDMI: 6.3] Video Format Timing Support"	"All specified video line pixel counts and video field line counts (both active and total) and HSYNC and VSYNC positions and durations shall be adhered to when transmitting a specified video format timing."
[861B: Chapter 4] VIDEO FORMATS AND WAVEFORM TIMINGS"	<See reference for details.>

Test Objective

Verify that Source DUT, whenever transmitting any EIA/CEA-861B-defined video format, complies with all required pixel and line counts and pixel clock frequency range.

Required Test Method

It is permitted for the ATC to not test formats listed in HDMI 6.3.2 as "Optional Video Formats". ATC testing is required to verify active and total counts for both horizontal and vertical as well as HSYNC and VSYNC polarity. The ATC may optionally verify all other parameters.

- Connect Source DUT to a Video Timing Analyzer.

For each format listed in CDF field

Field Name	***Field Definition***	***Choices***	***Repeater Mini-CDF***
Source_861B_Formats	Which EIA/CEA-861B video formats are supported by product?	861B format numbers (1…34)	2 (if 60Hz product) 17 (if 50Hz product)

- , perform the following.
- Operate Source DUT as required to output the tested format. For all of the following, refer to the values listed in Table 7-1 and Table 7-2 for the tested format.
- If CDF field Source_AVI_Required is 'Y':
  - Verify that an AVI InfoFrame is transmitted on every video field.
  - If any video field occurs with no AVI InfoFrame → FAIL
- With a frequency counter, measure the pixel clock rate.
- For any video format listed in Table 7-1 and Table 7-2 as 60Hz, 30Hz or 24Hz, pixel clock may be +0.5%/-0.6% of the listed pixel rate to allow for lower vertical rates than those listed (59.94Hz vs. 60Hz, etc.).
- If pixel clock is outside of allowable range → FAIL
- From beginning of capture data, scan for first Video Data Period in capture.
- Examine HSYNC and VSYNC values at last pixel before transition to Video Data Period.
- If HSYNC == 1 then HS_POLARITY = 0, else HS_POLARITY = 1
- If VSYNC == 1 then VS_POLARITY = 0, else VS_POLARITY = 1
- If either value HS_POLARITY or VS_POLARITY do not equal values for the selected video format → FAIL
- For each HSYNC active edge, examine all HSYNC and Video Data Periods to calculate following variables:
  - HS_LEN = number of pixels that HSYNC remains active
  - VIDEO_TO_HS = number of pixels from end of Video Data Period to HSYNC active edge
  - H_ACTIVE = number of pixels in Video Data Period minus 2 (for Guard Band)
  - H_TOTAL = number of pixels between two HSYNC active edges
  - If any value HS_LEN, HS_TO_VIDEO, H_ACTIVE and H_TOTAL do not equal values for the selected video format → FAIL
- Examine VSYNC/HSYNC relationship for two video fields.
- If VSYNC active edge alternates from field to field between coincident with HSYNC and mid-point between two HSYNC active edges then SCAN = INTERLACED
- If VSYNC is coincident with HSYNC on every field then SCAN = PROGRESSIVE
- For each VSYNC active edge, calculate following variables:
  - VS_LEN = number of pixels that VSYNC remains active divided by H_TOTAL, rounded to nearest half-integer (i.e. 6 or 6.5).

- V_ACTIVE = number of Video Data Periods between each two VSYNC active edges
- V_TOTAL = number of pixels between VSYNC active edges divided by H_TOTAL, rounded to nearest half-integer
- If SCAN == PROGRESSIVE, examine all VSYNC, HSYNC and Video Data Periods to calculate following variables
  - VS_TO_VIDEO = number of HSYNC pulses between VSYNC active edge and first subsequent Video Data Period, not including HSYNC pulse that is coincident (or nearly so) with VSYNC active edge
- If SCAN == INTERLACED, examine all VSYNC, HSYNC and Video Data Periods to calculate following variables:
  - VS_TO_VIDEO = number of HSYNC pulses between VSYNC active edge and first subsequent Video Data Period, not including (for Field 1) HSYNC pulse that is coincident (or nearly so) with VSYNC active edge or (for Field 2) HSYNC pulse following VSYNC edge by ½ line
- If any value VS_LEN, VS_TO_VIDEO, V_ACTIVE and V_TOTAL do not equal values for the selected video format → FAIL

- Determine 861B Video Code for the transmitted format. Note for subsequent tests.

Recommended Test Method

Setup Source DUT and Video Timing Analyzer and operate Source DUT as described above.

- HDMI Analysis command: ’Full HDMI Compliance‘ or ’Video Timing’
- If HDMI Analysis reports ‘PASS’, then PASS, else FAIL

861B Video Code	Format	Pixel Clock (MHz)	H_ TOTAL Pixels	H_ ACTIVE Pixels	VID_ TO_HS clocks	HS_ POLR'Y	HS_ LEN clocks
1	640x480p @ 60 Hz	25.2	800	640	16	-	96
2,3	720x480p @ 60 Hz	27.027	858	720	16	-	62
4	1280x720p @ 60 Hz	74.25	1650	1280	110	+	40
5	1920x1080i @ 60 Hz	74.25	2200	1920	88	+	44
6,7	720(1440)x480i @ 60 Hz	27.027	1716	1440	38	-	124
8,9	720(1440)x240p @ 60 Hz	27.027	1716	1440	38	-	124
10,11	2880x480i @ 60 Hz	54.054	3432	2880	76	-	248
12,13	2880x240p @ 60 Hz	54.054	3432	2880	76	-	248
14,15	1440x480p @ 60 Hz	54.054	1716	1440	32	-	124
16	1920x1080p @ 60 Hz	148.5	2200	1920	88	+	44
17,18	720x576p @ 50 Hz	27.0	864	720	12	-	64
19	1280x720p @ 50 Hz	74.25	1980	1280	440	+	40
20	1920 x 1080i @ 50 Hz	74.25	2640	1920	528	+	44
21,22	720(1440)x576i @ 50 Hz	27.0	1728	1440	24	-	126
23,24	720(1440)x288p @ 50 Hz	27.0	1726	1440	24	-	126
25,26	2880x576i @ 50 Hz	54.0	3456	2880	48	-	252
27,28	2880x288p @ 50 Hz	54.0	3456	2880	48	-	252
29,30	1440x576p @ 50 Hz	27.0	1728	1440	24	-	128
31	1920x1080p @ 50 Hz	148.5	2640	1920	528	+	44
32	1920x1080p @ 24 Hz	74.25	2750	1920	638	+	44
33	1920x1080p @ 25 Hz	74.25	2640	1920	528	+	44
34	1920x1080p @ 30Hz	74.25	2200	1920	528	+	44

Table 7-1 Video Format Timing – Horizontal and Clock Parameters

Regarding all 60Hz-class formats:

- Per-EIA/CEA-861B, all non-HDTV formats must be listed in the EDID at a 59.94Hz vertical frequency while HDTV formats must be listed as 60Hz. Note that pixel clock frequencies shown here all correspond to 60Hz frame rates, for ease and consistency in testing.
- Pixel clock may be +0.5%/-0.6% of the listed pixel rate to allow for lower vertical rates than those listed (59.94Hz vs. 60Hz, etc.).

861B Video Code	Format	V_ TOTAL (lines)	V_ ACTIVE (lines)	VS_ TO_VID (lines)	VS_ LEN (lines)	VS_ POLARITY	HV _OFFSET (pixels)
1	640x480p @ 60 Hz	525	480	35	2	-	0
2,3	720x480p @ 60 Hz	525	480	36	6	-	0
4	1280x720p @ 60 Hz	750	720	25	5	+	0
5	1920x1080i @ 60 Hz	562.5	540	20	5	+	0 / 1100
6,7	720(1440)x480i @ 60 Hz	262.5	240	18	3	-	0 / 858
8,9	720(1440)x240p @ 60 Hz	262 or 263	240	18	3	-	0
10,11	2880x480i @ 60 Hz	262.5	240	18	3	-	0 / 1716
12,13	2880x240p @ 60 Hz	262 or 263	240	18	3	-	0
14,15	1440x480p @ 60 Hz	525	480	36	6	-	0
16	1920x1080p @ 60 Hz	1125	1080	41	5	+	0
17,18	720x576p @ 50 Hz	625	576	44	5	-	0
19	1280x720p @ 50 Hz	750	720	25	5	+	0
20	1920 x 1080i @ 50 Hz	562.5	540	20	5	+	0 / 1320
21,22	720(1440)x576i @ 50 Hz	312.5	288	22	3	-	0 / 864
23,24	720(1440)x288p @ 50 Hz	312…314	288	22	3	-	0
25,26	2880x576i @ 50 Hz	312.5	288	22	3	-	0 / 1728
27,28	2880x288p @ 50 Hz	312…314	288	22	3	-	0
29,30	1440x576p @ 50 Hz	625	576	22	5	+	0
31	1920x1080p @ 50 Hz	1125	1080	41	5	+	0
32	1920x1080p @ 24 Hz	1125	1080	41	5	+	0
33	1920x1080p @ 25 Hz	1125	1080	41	5	+	0
34	1920x1080p @ 30Hz	1125	1080	41	5	+	0

Table 7-2 Video Format Timing – Vertical Parameters

Note: Interlaced formats alternate between HSYNC/VSYNC coincident and HSYNC/VSYNC offset by ½ line. The values in column HV_OFFSET above represent the HSYNC/VSYNC offset for each of the two repeating interlaced fields.

Note: It is permitted for the ATC to not test formats listed in HDMI 6.3.2 as “Optional Video Formats”. These formats are indicated in the tables above as:

	Primary Format
	Optional Format – Not required for ATC testing

Test ID 7-26: Pixel Repetition

Reference	Requirement
[HDMI: Table 8-3] HDMI Valid Pixel Repeat Values for Each Format	<See reference for details, summarized in Table 7-3, below.>

Test Objective

Verify that Source DUT indicates Pixel Repetition values in the AVI as required and that the pixels are actually repeated the indicated number of times.

Required Test Method

Connect Source DUT to a Video Timing Analyzer. For each format listed in CDF field

Field Name	***Field Definition***	***Choices***	***Repeater Mini-CDF***
Source_861B_Formats	Which EIA/CEA-861B video formats are supported by product?	861B format numbers (1…34)	2 (if 60Hz product) 17 (if 50Hz product)

, the following verifications shall be made.

These verifications assume that the Video Format Timing test has been executed and passed for the transmitted format and that the 861B Video Code has been determined.

- For the following, refer to the row in Table 7-3 corresponding to the transmitted video format timing.
- If no AVI is transmitted:
  - If column “No AVI Value” contains “illegal” → FAIL
  - If column “No AVI Value” contains the value 1 (meaning that the pixel is sent twice):
    - Examine each group of 2 video pixels in each Video Data Period. For each group (H_ACTIVE / 2):
      - Verify that both video pixels in group are identical. If they are different → FAIL
- If AVI is transmitted, examine PR value (PR = PR3*8 + PR2*4 + PR1*2 + PR0):
  - If PR value is not listed in column “Legal PR Values” → FAIL
  - If PR != 0:
    - Examine each group of PR+1 video pixels in each Video Data Period. For each group (H_ACTIVE / (PR+1)):
      - Verify that all PR+1 video pixels in group are identical. If any are different from the others → FAIL

Table 7-3 Pixel Repeat Values

861B Video Code	Video Description	No AVI Value	Legal PR Values
1	640x480p @ 60Hz	0	0
2,3	720x480p @ 59.94/60Hz	0	0
4	1280x720p @ 59.94/60Hz	0	0
5	1920x1080i @ 59.94/60Hz	0	0
6,7	720(1440)x480i @ 59.94/60Hz	1	1
8,9	720(1440)x240p @ 59.94/60Hz	1	1
10,11	2880x480i @ 59.94/60Hz	illegal	0, 1,…9
12,13	2880x240p @ 59.94/60Hz	illegal	0,1,…9
14,15	1440x480p @ 59.94/60Hz	illegal	0, 1
16	1920x1080p @ 59.94/60Hz	0	0
17,18	720x576p @ 50Hz	0	0
19	1280x720p @ 50Hz	0	0
20	1920x1080i @ 50Hz	0	0
21,22	720(1440)x576i @ 50Hz	1	1
23,24	720(1440)x288p @ 50Hz	1	1
25,26	2880x576i @ 50Hz	illegal	0,1,…9
27,28	2880x288 @ 50Hz	illegal	0,1,…9
29,30	1440x576p @ 50Hz	illegal	0, 1
31	1920x1080p @ 50Hz	0	0
32	1920x1080p @ 23.97/24Hz	0	0
33	1920x1080p @ 25Hz	0	0
34	1920x1080p @ 29.97/30Hz	0	0

Recommended Test Method

Setup Source DUT and P/A/V Analyzer and operate Source DUT as described above.

- HDMI Analysis command: ’Full HDMI Compliance‘ or ’Pixel Repetition’
- If HDMI Analysis reports ‘PASS’, then PASS, else FAIL

Test ID 7-27: AVI InfoFrame

Reference	Requirement
[HDMI: 8.2.1] Auxiliary Video Information	<See reference for details>
[861B: 6.1] Auxiliary Video Information (AVI) InfoFrame	"If the source device supports the transmission of the Auxiliary Video Information (AVI) and if it determines that the DTV Monitor is capable of receiving that information, it shall send the AVI to the DTV Monitor once per frame." "If no AVI is being sent from the source device, then the DTV Monitor shall assume the video data is RGB." "The information on 'Active Format Aspect Ratio,' bar widths, overscan/underscan, non-uniform picture scaling, and colorimetry is information that can be used by the DTV Monitor…If this information is present at the source device and valid…it is required that this information be sent."

Test Objective

Verify that an AVI InfoFrame is transmitted on every video field when required and that any AVI InfoFrame transmitted is accurate.

Required Test Method

- [Verify that CDF field Source_AVI_Required is set correctly]
- If CDF field Source_AVI_Required is 'N':
  - [AVI InfoFrame must be transmitted once per field whenever Source supports the transmission of the AVI InfoFrame.]
    - If CDF field Source_HDMI_YC_BC_R is 'Y' → FAIL
  - [AVI shall be sent when 2880x240, 288, 480 or 576-line format is transmitted or 1440x480p or 1440x576p. That is, formats 10-15 and 25-30. If Source is capable of transmitting any of these formats, it is required to transmit AVI.]

If CDF field

Field Name	***Field Definition***	***Choices***	***Repeater Mini-CDF***
Source_861B_Formats	Which EIA/CEA-861B video formats are supported by product?	861B format numbers (1…34)	2 (if 60Hz product) 17 (if 50Hz product)

- includes any of the following: 10, 11, 12, 13, 14, 15, 25, 26, 27, 28, 29, 30 → FAIL

- [AVI shall be sent when Source is transmitting any video format timing listed in EDID with multiple aspect ratios.]

If CDF field

Field Name	*Field Definition*	*Choices*	*Repeater Mini-CDF*
Source_861B_Formats	Which EIA/CEA-861B video formats are supported by product?	861B format numbers (1…34)	2 (if 60Hz product) 17 (if 50Hz product)

        - includes any of the following pairs: 2 and 3, 6 and 7, 8 and 9, 10 and 11, 12 and 13, 14 and 15, 17 and 18, 21 and 22, 23 and 24, 25 and 26, 27 and 28, or 29 and 30: → FAIL
    - [AVI shall be transmitted whenever the Active Format, Bar, Overscan/Underscan, Scaling, or Colorimetry information if available and valid at the Source.]
        - If CDF field Source_AVI_Info_Available is 'Y' → FAIL
    - [AVI InfoFrame shall be transmitted whenever the Source uses alternate colorimetry.
        - If CDF field Source_Alt_Colorimetry is 'Y' → FAIL
- If CDF field Source_AVI_Required == 'Y' and Source_AVI_Supported == 'N' → FAIL
- Connect Source DUT to a Video Picture Analyzer and operate as described in Section 7.4.1.
- [Verify that AVI InfoFrame is transmitted once per field if Source is required to use AVI InfoFrame]
    - If CDF field Source_AVI_Supported == 'Y':
        - If any video field occurs with no AVI InfoFrame → FAIL
- [Verify that only AVI InfoFrame v2 is transmitted (no v1 or other) whenever AVI InfoFrame is transmitted at all.]
- If no AVI is sent, Source shall only transmit that format in the Sink-preferred aspect ratio.
    - Attempt to configure Source to transmit video without corresponding AVI.
    - If no AVI sent in some configurations, verify that transmitted video corresponds to "Preferred" aspect ratio of Sink.
    - Transmitted video shall correspond to preferred aspect ratio of Sink.
- [AVI AR must describe video format in EDID and must match transmitted video format.]
    - Attempt to make Source DUT output video with each of its supported aspect ratios.
    - View image to determine transmitted aspect ratio and compare to AR information in AVI.
    - If AVI A, R or M fields do not correspond to viewed image → FAIL
- [Whenever transmitting an 861B-defined video format, any transmitted AVI InfoFrame, VIC field (Video Identification Code)must be non-zero and accurate.]
    - Attempt to make Source DUT output video using an 861B format.
    - If AVI VIC fields do not correspond to transmitted video format → FAIL
- [Whenever transmitting a non-861B-defined format, any transmitted AVI InfoFrame, VIC field must be zero.]
    - Attempt to make Source DUT output video using a non-861B format.

- If Source DUT capable and outputting a non-861B format:
- If AVI VIC fields are not all zero → FAIL

- All reserved fields in AVI InfoFrame shall be zero.

Recommended Test Method

Setup Source DUT and P/A/V Analyzer and operate Source DUT as described above.

- HDMI Analysis command: 'Full HDMI Compliance' or 'AVI InfoFrame'
- If HDMI Analysis reports 'PASS', then PASS, else FAIL

7.6 Source – Audio

7.6.1 Combinations of Audio and Video Formats

The following tests shall be performed at each of the following three combinations of video and audio formats. Note that the Audio Sample packet rate depends upon the audio sampling frequency, whether Layout 0 or Layout 1 is used and, if Layout 0, how many samples per packet are used. If Layout 0 is used, assume that four 2-channel audio samples are present in each packet.

- One of the Source-supported mandatory video formats (480p, 576p or 640x480p) and an audio format with the highest Audio Sample *packet* rate available.
- Any video format with the lowest supported line frequency and any audio format with the highest Audio Sample *packet* rate available
- An audio format with the highest Audio Sample *packet* rate available for the product using whatever video format is required to carry that audio format.

In many cases, one or more of these cases will overlap. In these cases, the tests do not need to be repeated.

7.6.2 Tests

Test ID 7-28: IEC 60958/IEC 61937

Reference	Requirement
[HDMI: 7.1] Relationship with IEC 60958/IEC 61937	<See reference for details.>

Test Objective

Verify that the behavior of all fields within the Audio Sample Subpackets follows the corresponding rules specified in the IEC 60958 or IEC 61937 specifications.

Required Test Method

If CDF field Source_Basic_Audio== 'N' then PASS

For the following: 2-channel audio samples are counted. For each Audio Sample packet, if Layout = 0, each audio sample is indicated by an SP bit. If Layout = 1, each Audio Sample packet represents one audio sample.

- Count audio samples between indicated B bit.
- If repetition period of B bit is not 192 "Frames" (2-channel samples) → FAIL

Recommended Test Method

If CDF field Source_Basic_Audio== 'N' then PASS

Setup Source DUT and P/A/V Analyzer and operate Source DUT as described above.

- HDMI Analysis command: 'Full HDMI Compliance' or 'Audio IEC Compliance'
- If HDMI Analysis reports 'PASS', then PASS, else FAIL

Test ID 7-29: ACR

Reference	Requirement
[HDMI: 6.3] Audio Sample Clock Capture and Regeneration	<See reference for details.>

Test Objective

Verify that the relationship between the parameters (N, CTS, audio sample rate) is correct with respect to the Audio Clock Regeneration mechanism.

Required Test Method

If CDF field Source_Basic_Audio== 'N' then PASS

- [Verify N parameter value.]
  - Get nominal sampling frequency (Fs) from the Channel/Status bits.
  - Get N parameter from ACR packet.
  - If $128*Fs/1500 \leq N \leq 128*Fs/300$ then continue test else → FAIL
- [Verify CTS parameter value.]
  - Monitor ACR Packets with "new" (non-zero) values of CTS
  - Measure the actual audio sample rate (Fs_actual).
  - Count the number of audio samples (n) over 2 seconds (Ts). Calculate Fs_actual using the following equation:
    - Fs_actual = n / Ts
  - Average the CTS values ($CTS_{average}$) over 2 seconds or more.
  - Measure the TMDS clock (f_{TMDS_clock}) with an accuracy of 1 ppm.
  - Get the nominal audio clock accuracy from the Channel/Status bits.
  - If clock accuracy == 50 ppm
    - if $CTS_{average}$ is within $(f_{TMDS\_clock} * N) / (128 * Fs) \pm 50$ ppm then continue test, else → FAIL
  - Else, if accuracy == 1000 ppm
    - if $CTS_{average}$ is within $(f_{TMDS\_clock} * N) / (128 * Fs\_actual) \pm 100$ ppm then continue test, else → FAIL
- [Verify CTS transmitting interval]
  - Monitor ACR Packets with "new" (non-zero) values of CTS
  - Average new CTS transmitting interval ($CTS_{interval}$) over 2 sec or more.
  - If $CTS_{interval} = N / (128 * Fs) \pm 2000$ppm then PASS else FAIL

Recommended Test Method Test ID 7-29: ACR

If CDF field Source_Basic_Audio== 'N' then PASS

Setup Source DUT and P/A/V Analyzer and operate Source DUT as described above.

- HDMI Analysis command: 'Full HDMI Compliance' or 'ACR'
- If HDMI Analysis reports 'PASS', then PASS, else FAIL

Test ID 7-30: Audio Sample Packet Jitter

Reference	Requirement
[HDMI: 7.8.1] Audio Sample Packets	<See reference for details.>

Test Objective

Verify that the source audio packet jitter is within the limits specified.

Required Test Method

If CDF field Source_Basic_Audio== 'N' then PASS

- [Verify audio packet jitter]
  - Measure actual audio sample rate (Fs_actual).
    - n = number of audio samples over 2 seconds or more (= Ts).
    - Calculate Fs_actual using the following equation:
    - Fs_actual = n / Ts
  - If audio packet jitter relative to actual sampling rate does not exceed one video horizontal line period plus a single audio sample period then PASS else FAIL

Recommended Test Method

If CDF field Source_Basic_Audio== 'N' then PASS

Setup Source DUT and P/A/V Analyzer and operate Source DUT as described above.

- HDMI Analysis command: 'Full HDMI Compliance' or 'Audio Packet Jitter'
- If HDMI Analysis reports 'PASS', then PASS, else FAIL

Test ID 7-31: Audio InfoFrame

Reference	Requirement
[861B: 6.3] Audio InfoFrame	"If the source device supports the transmission of the Audio InfoFrame and if it determines that the DTV Monitor is capable of receiving…digital audio, then the Audio InfoFrame, with Data Bytes 1 through 3 set correctly, shall be sent once per video frame while digital audio is being sent across the interface."
[861B: 6.3.1] Audio Identification Information	"If the DTV and the source device support more than "basic audio," as defined by the physical/link specification, then this information shall be sent and shall accurately identify the stream while digital audio is being sent."

Test Objective

Verify that Source transmits an Audio InfoFrame whenever required and that contents are valid.

Required Test Method

If CDF field Source_Basic_Audio== 'N' then PASS

- [Check Audio InfoFrame placement]
- Examine the placement of the Audio InfoFrame Packet
- If Audio InfoFrame Packet is detected at least once per video field then continue else → FAIL
- [Check Packet Header]
- If Packet Header has the following contents
  - HB0: 0x84 (InfoFrame Type Code=0x00~0x7F)
  - HB1: 0x01
  - HB2: 0x0A (InfoFrame_length >=0x1B, max)
  - Then continue else → FAIL:
- [Check Packet Body]
- Read Packet Body (PB0 to PB27)
- [Check PB1 to PB5]
  - if the value of Audio Coding Type (CT3~CT0) is 0x0 then continue else → FAIL
  - If the value of bit 3 is zero then continue else → FAIL.
  - If the value of the most significant three bits of PB2 is zero then continue else → FAIL.
  - If the value of Sampling Frequency (SF2~ SS0) is zero then continue else → FAIL.
  - If the value of Sample Size (SS1~ SS0) is Zero. then continue else → FAIL.
- [Check for illegal CA]
  - If CA > 0x20 then FAIL
- [Check for valid Combination of (CA7 ~ CA0) and (CC2 ~ CC0)]

- If indicator in Audio sample packet indicates layout 0
  - If CC== 0,0,0 or CC == 0,0,1 and CA== 0x00 then continue else → FAIL
- else [layout 1]
  - FAIL if any of the below statements are false:
    CC== 0,0,0 and CA is in set { 0x01,0x02,0x03,…, 0x1F }
    CC== 0,1,0 and CA is in set { 0x01, 0x02 or 0x04 }
    CC== 0,1,1 and CA is in set { 0x03, 0x05, 0x06, 0x08 or 0x14}
    CC== 1,0,0 and CA is in set { 0x07, 0x09, 0x0A, 0x0C, 0x15, 0x16, 0x18 }
    CC== 1,0,1 and CA is in set { 0x0B, 0x0D, 0x0E, 0x10, 0x17, 0x19, 0x1A , 0x1C }
    CC== 1,1,0 and CA is in set { 0x0F, 0x11, 0x12, 0x1B, 0x1D or 0x1E }
    CC== 1,1,1 and CA is in set { 0x13 or 0x1F }

- [If LSV is non-zero, then only 2-channels allowed (downmix)]
  - If LSV != 0x0 and CA != 0x00 then → FAIL
- [Check for valid combination of DM_INH and CA]
  - If DM_INH ==1 and CA == 0x00 then → FAIL
- If value of the least significant three bits of PB5 is zero then continue else → FAIL
- If value of PB6 through PB27 is 0x00. then continue else → FAIL
- [Verify checksum]
- Do a byte wide sum of HB0,HB1,HB2, PB0, PB1, PB2,…, PB10.
- If sum == 0x00 then PASS else → FAIL

Recommended Test Method

Setup Source DUT and P/A/V Analyzer and operate Source DUT as described above.

- HDMI Analysis command: ’Full HDMI Compliance‘ or ’Audio InfoFrame’
- If HDMI Analysis reports ‘PASS’, then PASS, else FAIL

Test ID 7-32: Audio Sample Packet Layout

Reference	Requirement
[HDMI:7.6] Audio Data Packetization	See reference
[861B: 6.3.1] Audio Identification Information	"If the DTV and the source device support more than "basic audio," as defined by the physical/link specification, then this information shall be sent and shall accurately identify the stream while digital audio is being sent."

Test Objective

Verify that Source only transmits audio using permitted Layout type.

Required Test Method

- Read HB1 and HB2 from header
- If Audio Sample Packet Layout == 0 (Bit 4 of HB1)
  - [check for valid combinations of Sample Present and B]
  - Use the following table to check for a valid combination of Sample present and B values contained within HB1 and HB2.
  - If combination contained in HB1 & HB2 is not in this table then → FAIL

Sample Present	B
0000	0000
0001	000x
0011	00bb
0111	0bbb
1111	bbbb

Where:

Sample Present is bits 3..0 of HB1

B is bits 7..4 of HB2

x is don't care

b don't care, but only 1 bit may be set

- If Audio Sample Packet Layout = 1 (Bit 4 of HB1).
  - [Check for valid combinations of Channel Allocation (CA), Sample Present and B]
  - Read CA from PB4 of Audio Info Frame
  - Use the following table to check for a valid combination of CA, Sample present and B values.
  - If combination is not in this table then → FAIL

CA								Sample Present				B			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**3**	**2**	**1**	**0**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	1	0	0	SP	SP	0	0	x	x
0	0	0	0	0	0	1	0	0	0	SP	SP	0	0	x	x
0	0	0	0	0	0	1	1	0	0	SP	SP	0	0	x	x
0	0	0	0	0	1	0	0	0	SP	0	SP	0	x	0	x
0	0	0	0	0	1	0	1	0	SP	SP	SP	0	x	x	x
0	0	0	0	0	1	1	0	0	SP	SP	SP	0	x	x	x
0	0	0	0	0	1	1	1	0	SP	SP	SP	0	x	x	x
0	0	0	0	1	0	0	0	0	SP	0	SP	0	x	0	x
0	0	0	0	1	0	0	1	0	SP	SP	SP	0	x	x	x
0	0	0	0	1	0	1	0	0	SP	SP	SP	0	x	x	x
0	0	0	0	1	0	1	1	0	SP	SP	SP	0	x	x	x
0	0	0	0	1	1	0	0	SP	SP	0	SP	x	x	0	x
0	0	0	0	1	1	0	1	SP	SP	SP	SP	x	x	x	x
0	0	0	0	1	1	1	0	SP	SP	SP	SP	x	x	x	x
0	0	0	0	1	1	1	1	SP	SP	SP	SP	x	x	x	x
0	0	0	1	0	0	0	0	SP	SP	0	SP	x	x	0	x
0	0	0	1	0	0	0	1	SP	SP	SP	SP	x	x	x	x
0	0	0	1	0	0	1	0	SP	SP	SP	SP	x	x	x	x
0	0	0	1	0	0	1	1	SP	SP	SP	SP	x	x	x	x
0	0	0	1	0	1	0	0	SP	0	0	SP	x	0	0	x
0	0	0	1	0	1	0	1	SP	0	SP	SP	x	0	x	x
0	0	0	1	0	1	1	0	SP	0	SP	SP	x	0	x	x
0	0	0	1	0	1	1	1	SP	0	SP	SP	x	0	x	x
0	0	0	1	1	0	0	0	SP	SP	0	SP	x	x	0	x
0	0	0	1	1	0	0	1	SP	SP	SP	SP	x	x	x	x
0	0	0	1	1	0	1	0	SP	SP	SP	SP	x	x	x	x
0	0	0	1	1	0	1	1	SP	SP	SP	SP	x	x	x	x
0	0	0	1	1	1	0	0	SP	SP	0	SP	x	x	0	x
0	0	0	1	1	1	0	1	SP	SP	SP	SP	x	x	x	x
0	0	0	1	1	1	1	0	SP	SP	SP	SP	x	x	x	x
0	0	0	1	1	1	1	1	SP	SP	SP	SP	x	x	x	x

Where:

x = any value

SP = any value, but all SP must be same

Recommended Test Method

Setup Source DUT and P/A/V Analyzer and operate Source DUT as described above.

- HDMI Analysis command: 'Full HDMI Compliance' or 'Audio Layout'
- If HDMI Analysis reports 'PASS', then PASS, else FAIL

7.7 Source – Interoperability With DVI

Test ID 7-33: Interoperability With DVI

Reference	Requirement
[HDMI: App. C.1] Requirement for DVI Compatibility	"…all HDMI Sources shall be compatible with DVI 1.0 compliant sinks (i.e. "systems" or "hosts") through the use of a similar cable converter."
[HDMI: App. C.2] HDMI Source Requirements	"An HDMI Source, upon power-up, reset or detection of a new sink device, shall assume that the sink device operates under DVI 1.0 limitations. An HDMI Source shall determine if the sink device is an HDMI Sink by following the rule(s) described in Section 8.3.3. Upon detection of an HDMI Sink, the HDMI Source shall follow all of the HDMI Source-related requirements specified in this document."

Test Objective

Verify that Source never outputs a Video Guard Band or Data Island to a device without an HDMI VSDB.

Required Test Method

- Connect Source DUT to Protocol Analyzer with EDID that has no HDMI VSDB.
- If (any video transmitted) AND (no Guard Bands) AND (No data islands) → PASS
- If (any video transmitted) AND (any Guard Bands transmitted) → FAIL
- If (any video transmitted) AND (any Data Islands transmitted) → FAIL

8 Tests – Sink

8.1 Sink Products Overview

8.1.1 Television and Other Display Products

Display products are defined to “adequately support” a particular video format if they display that format, legibly and correctly placed (e.g. centered) horizontally and vertically in the expected aspect ratio and over/underscan amount.

For overscanned formats, horizontally and vertically, at least some portion of the active portion of the image must not be visible due to border obstruction or clipping. For underscanned images, 100% of the active portion must be visible.

8.1.2 Audio Rendering Products

Displays, audio amplifiers or other products designed to “render” the audio (convert to actual sound) are defined to “adequately support” a particular audio format if they reproduce the audio at approximately the same level of fidelity as any other audio input on that device.

8.1.3 Non-Display Devices

If the Sink product has no display but does have an analog or other video output that can be attached to a display thereby providing the same function, this output/display may be used to determine support of the received HDMI signal.

8.2 Sink – EDID / E-DDC

Test ID 8-1: EDID Readable

Reference	Requirement
[HDMI: 8.3] E-EDID Data Structure	"All Sinks shall contain an EIA/CEA-861B compliant E-EDID data structure accessible through the DDC." <See reference for additional details.>

Test Objective

Verify that the entire EDID is able to be read.

Required Test Method

- Connect an EDID Reader/Analyzer to the Sink DUT.
- Power ON the Sink DUT.
- Apply +5.0V to +5V Power pin.
- Operate the EDID Reader/Analyzer to perform the following:
  - Read Block 0 (128 bytes) of the Sink's EDID.
  - EXTENSION_COUNT = Extension Flag (block 0, byte 0x7E)
  - If EXTENSION_COUNT == 0x00 then:
    - FAIL → "Missing EDID Extension"
  - If EXTENSION_COUNT >= 0x01 then:
    - Use any sequence of legal DDC reads to read the second 128 bytes of the EDID.
    - If any read NACKs inappropriately → FAIL, "DDC NACK"
  - If EXTENSION_COUNT > 0x01 then:
    - Use any sequence of legal segment register-based E-DDC reads to read block 2 through block EXTENSION_COUNT+1
    - If any read NACKs inappropriately → FAIL, "E-DDC NACK"
- Store the EDID image for analysis on subsequent Sink tests.
- Power OFF the Sink DUT, continue applying +5.0V to +5V Power
- If HPD is asserted by Sink perform the following:
  - Read the entire EDID (as above)
  - If EDID image read error → FAIL
  - Compare to previously stored EDID image
  - If EDID images do not match → FAIL

Recommended Test Method Test ID 8-1: EDID Readable

- Connect Sink DUT to Silicon Image EDID Reader/Analyzer. Run EDID Analysis software and execute command “Read from DDC”, followed by “Save As…”. Save file in an appropriate location. This text file will be part of the Test Results Form.
- If any errors are reported during EDID read → FAIL, <error comment>
- Else, → PASS

Test ID 8-2: EDID VESA Structure

Reference	Requirement
[HDMI: 8.3] E-EDID Data Structure	"The first 128 bytes of the E-EDID shall contain an EDID 1.3 structure. The contents of this structure shall also meet the requirements of EIA/CEA-861B." <See reference for additional details.>
[861B: 7] EDID Data Structure	<See reference for details.>

Test Objective

Verify that the data in the base EDID 1.3 block and basic EDID Extension handling is correct and meets all aspects of the relevant specifications.

Required Test Method

Use the EDID Reader/Analyzer to analyze the EDID image that was captured in the "EDID Readable" above, as follows:

- EXTENSION_COUNT = Extension Flag (block 0, byte 0x7E)
- If EXTENSION_COUNT == 1
    - BLOCK_COUNT = 2
- Else, (EXTENSION_COUNT > 1)
    - BLOCK_COUNT = EXTENSION_COUNT+1
- Perform the following tests on Block 0:
    - [Verify valid EDID Block 0 header]
        - Examine block 0: bytes 0x00 through 0x07. Values shall be 0x00, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00.
        - If any values different → FAIL, "Incorrect Block 0 header"
    - [Verify EDID Version]
        - Examine bytes 0x12 and 0x13. Values shall be 0x01, 03h.
        - If any values different → FAIL, "Incorrect EDID version"
    - [Verify Video Information Byte] (This indicates that the interface is digital.)
        - Examine byte 0x14. Value shall be either 0x80 or 0x81.
        - If value is not 0x80 or 0x81 → FAIL, "Incorrect Video Information Byte"
    - [Verify Preferred Timing bit is set]
        - If byte 0x18, bit # 1 != 1→ FAIL, "Incorrect Preferred Timing bit"
    - [Verify that Detailed Timing Description #1 contains Preferred Timing]
        - Examine 16-bits at bytes 0x36 and 0x37. (Pixel clock / 10,000). Combined word shall be non-zero.

- If value is 0x0000 → FAIL, “Missing Preferred Timing descriptor”
- [Verify that Detailed Timing Descriptions #1-#4 contains one Monitor Range Limits descriptor and one Monitor Name descriptor]. [EDID 1.3: 3.10.3]
  - Examine 4 byte values at locations 0x36…0x39, 0x48…0x4B, 0x5A…0x5D and 0x6C…0x6F, looking for following values:
    - 0x00, 0x00, 0x00, 0xFD [= Monitor Range Limits header]
    - 0x00, 0x00, 0x00, 0xFC [= Monitor Name header]
  - If Monitor Range Limits header not present in examined bytes → FAIL, “Missing Monitor Range Limits”
  - If Monitor Name header not present in examined bytes → FAIL, “Missing Monitor Name”
- [Verify that Detailed Timing Descriptions #2, #3, or #4 appear in correct order]
  - If bytes 0x6C…0x6D != 0 or 0x5A…0x5B != 0 → FAIL, “DTD follows Monitor Descriptor”
  - If bytes 0x48…0x49 != 0 :
    - If bytes 0x36…0x37 == 0 → FAIL, “DTD follows Monitor Descriptor”

- [Verify that Block 1 contains either a CEA Timing Extension or a valid block map]
  - If EXTENSION_COUNT == 1
    - If block 1: byte 0 != 0x02 → FAIL, “Missing CEA T.E. in block 1”
  - Else, (EXTENSION_COUNT > 1)
    - If block 1: byte 0 != 0xF0 → FAIL, “Missing Block Map in block 1”
    - If block 2: byte 0 != 0x02 → FAIL, “Missing CEA T.E. in block 2”
    - For every byte <N> from byte 1 through byte EXTENSION_COUNT-1:
      - If block 1, byte N != block N+1, byte 0 → FAIL, “Block Map/Extension mis-match”
    - For every byte <N> from byte EXTENSION_COUNT through byte 0x7E (126):
      - If block 1, byte N != 0 → FAIL, “Block Map byte <N> incorrect”
- Perform the following for each block <N> in the EDID, from block 0 to block BLOCK_COUNT:
  - [Verify Block Checksum]
    - Sum all of the bytes in block from byte 0x00 to 0x7F. Result is the lower 8 bits of the sum. Sum result shall be 0x00.
    - If checksum != 0x00 → FAIL, “Incorrect checksum, block <N>”

Recommended Test Method Test ID 8-2: EDID VESA Structure

- If any errors are reported during EDID read → FAIL, <error comment>
- Following is assuming that EDID image has already been downloaded to PC running EDID Analysis software.
- Launch EDID Analysis tool and open the EDID image saved above in Test: “EDID Readable”.
- Execute EDID Analysis command “HDMI Analysis”.
- If any errors are reported → FAIL, <error comment>
- Else, → PASS

Test ID 8-3: CEA Timing Extension Structure

Reference	Requirement
[HDMI: 8.3.1] EDID Timing Extension	"The first E-EDID 'extension' shall contain a CEA EDID Timing Extension version 3, defined in EIA/CEA-861B section 7.5. Additional CEA EDID Timing Extensions may also be present." <See reference for additional details.>

Test Objective

Verify that the data in any CEA Timing Extension present in EDID is formatted properly and meets all aspects of the relevant specifications. [Note: The accuracy of the video and audio-related EDID information is tested in the Video and Audio test sections.]

Required Test Method

Use the EDID Reader/Analyzer to analyze the EDID image that was captured in the "EDID Readable" above, as follows:

- EXTENSION_COUNT = Extension Flag (block 0, byte 0x7E)
- If EXTENSION_COUNT == 1
  - BLOCK_COUNT = 2
- Else, (EXTENSION_COUNT > 1)
  - BLOCK_COUNT = EXTENSION_COUNT+1
- Perform following tests for each CEA T.E. found, including the first:
  - [Verify Version Number]
    - Check byte #2 of this CEA Timing Extension
    - If byte #2 != 3 → FAIL, "Incorrect CEA T.E. version"
  - [Verify data structure of CEA T.E.]
    - Scan through all Data Blocks checking the following:
      - If Data Block Tag Code (bits #7…5 of Data Block's 1st byte) has a value of 0, 5, 6, or 7 → FAIL, "Illegal Data Block type"
      - If Tag Code == 1 [Audio Data Block]
        - If 1st CEA Timing Extension byte #3, bit #6 is 0 → FAIL, "No Basic Audio but Audio Data Block found"
        - If Data Block Length (bits #4…0 of 1st byte) isn't a multiple of 3 (3, 6, 9…) → FAIL, "Illegal Audio Block length"
        - For each Short Audio Descriptor (3 bytes long) in Audio Data Block
          - If 1st byte, bit #7==1 or 2nd byte, bit #7==1 → FAIL, "Short Audio Descr. Rsvd bits set"
          - If Audio Format Code (1st byte, bits #6…3) == 0001 and 3rd byte != 0 → FAIL, "Short Audio Descr, Rsvd byte set"

- If Tag Code == 4 [Speaker Allocation Data Block]
  - If Data Block Length (bits #4…0 of 1st byte) != 3 → FAIL, "Illegal Speaker Alloc Block length"
  - If 1st byte of Speaker Allocation Data Block Payload, bit #7==1 → FAIL, "Speaker Alloc Descr. rsvd bits set"
  - If 2nd byte!=0 or 3rd byte!=0 → FAIL, "Speaker Alloc. rsvd bytes set"
  - Verify that only 1 Speaker Allocation Data Block is present and in 1st CEA T.E.
  - Verify that a Speaker Allocation Data Block is present if multi-channel audio is supported. [861B: 7.1.3] "If the DTV Monitor supports multi-channel LPCM (i.e., more than two channels), then it shall include the Speaker Allocation Data Block in the CEA EDID Timing Extension."
- If location of next Data Block (current location + 1 + length) < d, continue scanning of Data Blocks
- If location of next Data Block > d → FAIL, "d points into Data Block"
- If location of next Data Block == d, stop scanning and continue tests

- [Verify that starting with 1st DTD with 00 as pixel clock frequency, only filler bytes (0) follow until Checksum byte]
  - Following byte 'd', scan for 1st DTD with 0 in 1st two bytes. Scan all remaining bytes up to and including byte #126.
  - If any bytes != 0 → FAIL, "Non-zero value in padding"

- Perform the following for the 1st CEA Timing Extension in EDID:
  - [Verify presence of HDMI Vendor-Specific Data block in first CEA Timing Extension]
    - Find first Data block with the values 0b011xxxxx, 0x03, 0x0C, 0x00 in the first 4 bytes (where 'xxxxx' can be any 5 bit value).
    - If no Data Block in 1st CEA T.E. has signature above → FAIL, "Missing HDMI VSDB"
    - If first byte != 0x65 → FAIL, "HDMI VSDB incorrect length"
  - [Verify Physical Address in HDMI VSDB is X.0.0.0 for non-Repeater, where X is equal to the number of the port]
    - If CDF field CDF_HDMI_output_count == 0
      - If last two bytes of HDMI VSDB are not 0xX0 and 0x00 → FAIL, "Bad Physical Address"
  - [Verify that no HDMI VSDB exists in subsequent data block]
    - Search for a 2nd Data block with the values 0b011xxxxx, 0x03, 0x0C, 0x00 in the first 4 bytes.
    - If any other Data Block has signature above → FAIL, "Extra HDMI VSDB"
- Perform the following for all CEA T.E. except the 1st CEA T.E. in EDID:
  - [Verify consistency of byte 3 (number of preferred timings plus flags) among all CEA Timing Extensions]
    - Compare byte #3 of this CEA Timing Extension with byte #3 of first CEA Timing Extension.

- If byte 3 != byte 3 of 1st CEA T.E. → FAIL, “Unmatched byte 3 in CEA T.E.”

- [Verify that no HDMI VSDB exists in subsequent T.E.]
  - Search for a Data block with the values 0b011xxxxx, 0x03, 0x0C, 0x00 in the first 4 bytes.
  - If any Data Block in this CEA T.E. has signature above → FAIL, “Extra HDMI VSDB”

- [Verify that number of native (preferred) DTDs is ≤ number of DTDs in EDID]
  - If lower 4 bits of byte 3 of 1st CEA T.E. > number of DTDs in EDID → FAIL, “Too many preferred”

Recommended Test Method Test ID 8-3: CEA Timing Extension Structure

- Following is assuming that EDID image has already been downloaded to PC running EDID Analysis software.
- Launch EDID Analysis tool and open the EDID image saved above in Test: “EDID Readable”.
- Execute EDID Analysis command “HDMI Analysis”.
- If any errors are reported → FAIL, <error comment>
- Else, → PASS

8.3 Sink – Electrical

Test ID 8-4: TMDS – Termination Voltage

Reference	Requirement
[HDMI: Table 4-15 Sink DC Characteristics When Source Disabled or Disconnected at TP2	With Source disabled or disconnected, the differential voltage level on each TMDS pair must be AV_{CC}±10mV.

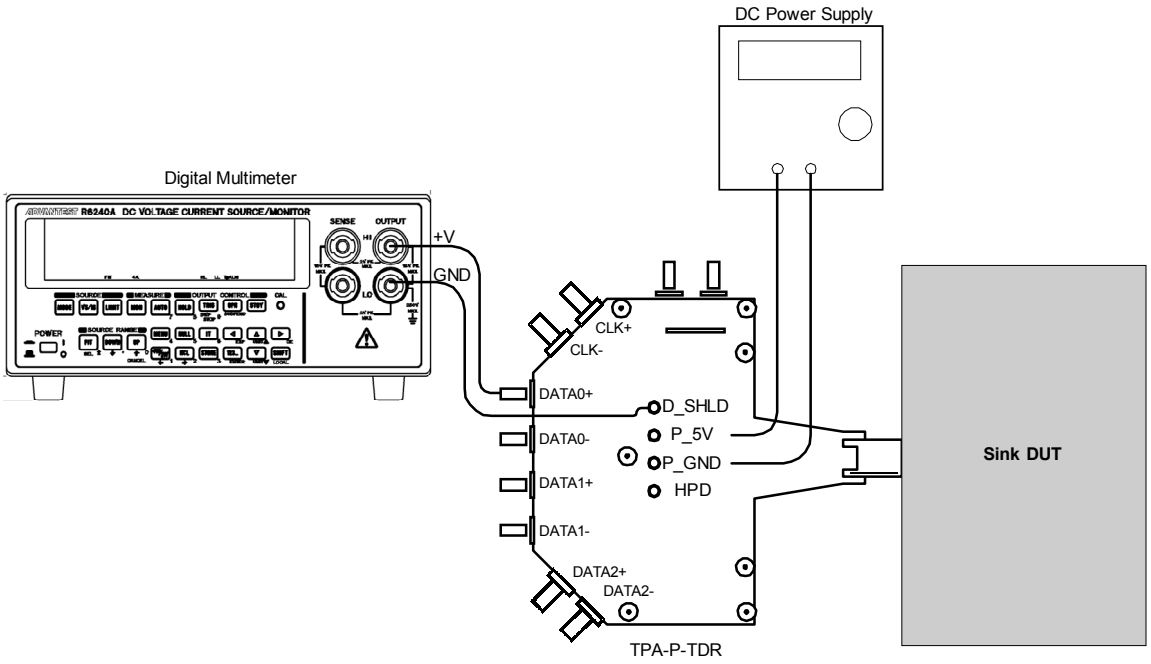
Test Objective

Confirm that the differential voltage level on each TMDS pair is within specified limits.

Required Test Method

- Connect TPA-P to HDMI input connector of Sink DUT.
- Turn on the power to the Sink DUT and verify that the HDMI input is active (e.g. correct input is selected, etc.).
- Connect the multi-meter probes to the TMDS_DATA0+ and TMDS_DATA0_Shield.
- V_{TERM} = measured voltage level
- If (V_{TERM} < 3.125V) OR (V_{TERM} > 3.475V) then FAIL.
- Repeat for all remaining TMDS_DATA and TMDS_CLOCK, + and - signals, measuring between the signal and its shield.

Recommended Test Method Test ID 8-4: TMDS – Termination Voltage



Setup 19. Test ID 8-4: TMDS – Termination Voltage

No.	Description	Recommended TE	Reference	Qty.
1	Digital Multi-Meter	ADVANTEST R6240A	4.2.1.11	1
2	DC Power Supply	KENWOOD PW18-1.8AQ	4.2.1.14	1
3	TPA-P-TDR Fixture	Tektronix TPA-P-TDR	4.2.1.1.6	1

- Connect TPA-P-TDR to HDMI input connector of Sink DUT.
- Verify that TPA-P-TDR has no termination resistors attached.
- Connect and configure DC Power Supply to drive +5V between +5V Power (P_5V) and DDC/CEC Ground (P_GND) on TPA-P-TDR
- Turn on the power to the Sink DUT and verify that the HDMI input is active (e.g. correct input is selected, etc.).
- Connect the multi-meter probes to the TMDS_DATA0+ and TMDS_DATA0_Shield.
- V_{TERM} = measured voltage level
- If (V_{TERM} < 3.125V) OR (V_{TERM} > 3.475V) then FAIL.
- Repeat for all remaining TMDS_DATA and TMDS_CLOCK, + and - signals, measuring between the signal and its shield.

Test ID 8-5: TMDS – Minimum Differential Sensitivity

Reference	Requirement
[HDMI: Table 4-16] Sink AC Characteristics at TP2	Minimum differential sensitivity (peak-to-peak) is 150mV.

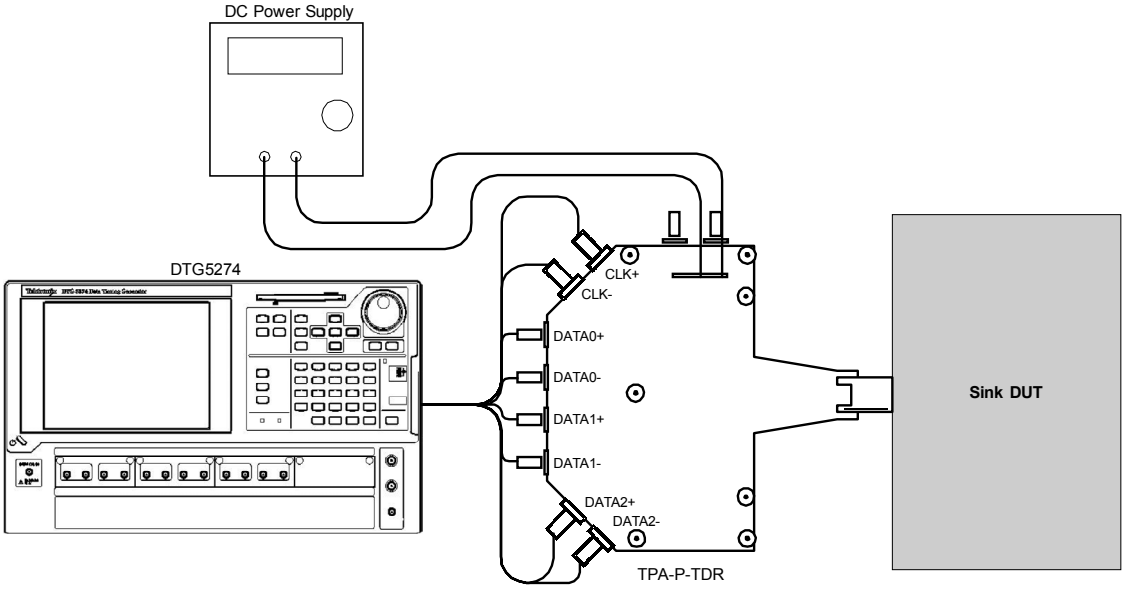
Test Objective

Confirm that the Sink properly supports TMDS differential voltages at minimum levels.

Required Test Method

- Connect TMDS Signal Generator to Sink DUT.
- Turn on the power to the Sink DUT and verify that the HDMI input is active.
- Configure the DTG to output any Sink-supported 27MHz video format.
- [Search for and record the minimum differential swing voltage that the Sink DUT supports without error at V_{ICM} = 3.0V]:
  - If V_{DIFF}{minimum} >= 150mV → FAIL.
- Repeat test for V_{ICM} = 3.13V.

Recommended Test MethodTest ID 8-5: TMDS – Minimum Differential Sensitivity



Setup 20. Test ID 8-5: TMDS – Minimum Differential Sensitivity

No.	Description	Recommended TE	Reference	Qty.
1	Digital Timing Generator (DTG)	Tektronix DTG5274	4.2.1.2	1
2	DC Power Supply	KENWOOD PW18-1.8AQ	4.2.1.14	1
3	SMA Cables	<See reference>	4.2.1.6	8
4	TPA-P-TDR Fixture	Tektronix TPA-P-TDR	4.2.1.1.6	1

- Connect DTG to TPA-P-TDR using eight 1 meter or 1.5 meter SMA cables:
  - Module A, Channel 1+, 1-: No connect
  - Module A, Channel 2+, 2-: No connect
  - Module B, Channel 1+, 1-: connect to TMDS_DATA0+,– (DATA0_P, DATA1_N)
  - Module B, Channel 2+, 2-: connect to TMDS_DATA1+,–
  - Module C, Channel 1+, 1-: connect to TMDS_DATA2+,–
  - Module C, Channel 2+, 2-: connect to TMDS_CLOCK+,–
- Connect HDMI plug of TPA-P-TDR to HDMI input connector of Sink DUT.
- Connect and configure DC Power Supply to drive +5V between +5V Power (P_5V) and DDC/CEC Ground (P_GND) on TPA-P-TDR.
- Turn on the power to the Sink DUT and verify that the tested input is active.
- Configure the DTG to output any Sink-supported 27MHz video format.
  - Repeating RGB gray ramp 0, 1, 2…254, 255, 0, 1, 2…during each video period

- [Search for and record the minimum differential swing voltage that the Sink DUT supports without error at V_{ICM} = 3.0V]:
  - Set V_{ICM} = 3.0V
  - Set V_{DIFF} = 170mV on all TMDS differential pairs. (Note that “Amplitude and Offset” mode in the DTG “Level” window should be chosen. In this mode, “Amplitude” should be set to 0.085Vpp to correspond to a 170mV differential swing.)
  - Reduce V_{DIFF}, in 20mV steps (corresponding to 0.01Vpp steps in the “Amplitude” setting), on all pairs until the Sink DUT outputs errors or V_{DIFF} of 70mV is reached.
  - Record V_{DIFF}{minimum} at first voltage level where errors appear.
  - If V_{DIFF}{minimum} >= 150mV → FAIL.
- Repeat test for V_{ICM} = 3.13V.

Test ID 8-6: TMDS – Intra-Pair Skew

Reference	Requirement
[HDMI: Table 4-16] Sink AC Characteristics at TP2	Allowable Intra-Pair Skew at Sink Connector is $0.4*T_{BIT}$

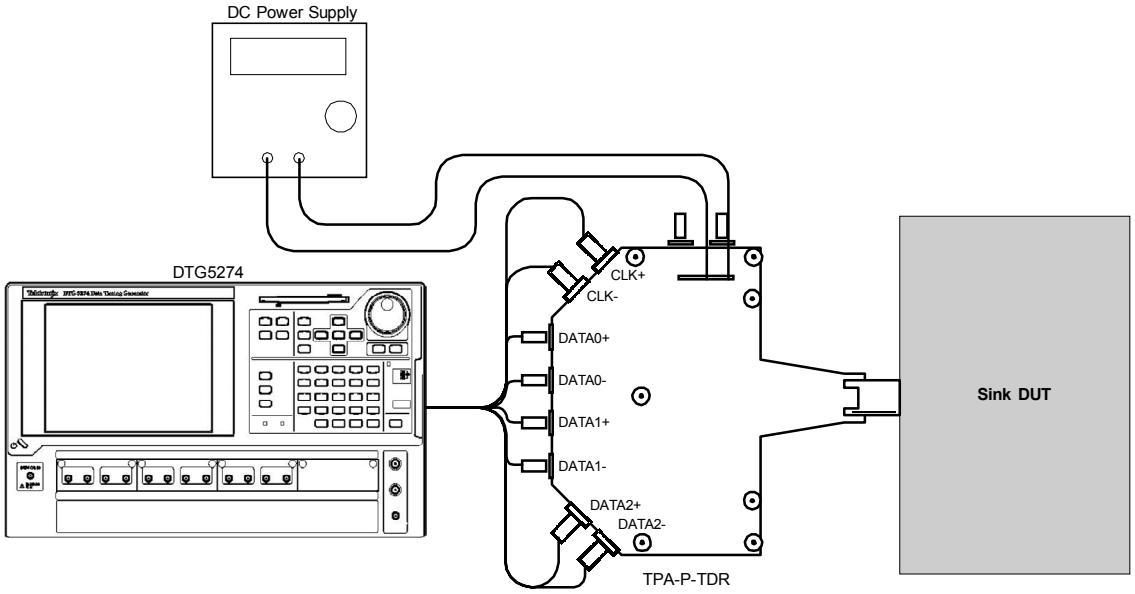
Test Objective

Confirm that the maximum allowed timing skew within each TMDS pair is supported by the Sink DUT.

Required Test Method

- Configure the TMDS Signal Generator to output any Sink-supported video format with the maximum Sink-supported pixel clock frequency.
- Connect TPA-P to HDMI input connector of Sink DUT.
- For each of the TMDS clock and data pairs acting as the tested pair:
  - Increase the skew (Differential Timing Offset) by steps of less than or equal to $0.1*T_{BIT}$, until the Sink DUT outputs errors or until reaching $0.6*T_{BIT}$ or 1nsec.
  - If errors seen on DUT:
    - Reduce the skew one step, so that Sink DUT outputs no errors.
    - If intra-pair skew < $0.4*T_{BIT}$, → FAIL.
- Repeat the test for each of the remaining untested pairs.

Recommended Test Method Test ID 8-6: TMDS – Intra-Pair Skew



Setup 21. Test ID 8-6: TMDS – Intra-Pair Skew

No.	Description	Recommended TE	Reference	Qty.
1	Digital Timing Generator (DTG)	Tektronix DTG5274	4.2.1.2	1
2	DC Power Supply	KENWOOD PW18-1.8AQ	4.2.1.14	1
3	SMA Cables	<See reference>	4.2.1.6	8
4	TPA-P-TDR Fixture	Tektronix TPA-P-TDR	4.2.1.1.6	1

- Connect DTG to TPA-P-TDR using eight 1 meter (preferable) or 1.5 meter SMA cables:
  - Module A, Channel 1+, 1-: No connect
  - Module A, Channel 2+, 2-: No connect
  - Module B, Channel 1+, 1-: connect to TMDS_DATA0+,–
  - Module B, Channel 2+, 2-: connect to TMDS_DATA1+,–
  - Module C, Channel 1+, 1-: connect to TMDS_DATA2+,–
  - Module C, Channel 2+, 2-: connect to TMDS_CLOCK+,–
- Connect TPA-P-TDR to HDMI input connector of Sink DUT.
- Connect and configure DC Power Supply to drive +5V between +5V Power (P_5V) and DDC/CEC Ground (P_GND) on TPA-P-TDR.
- Configure the TMDS Signal Generator to output any Sink-supported video format that uses the maximum Sink-supported pixel clock frequency. If multiple formats are available, a native format is preferred. Note the tested format on the results form.
  - Repeating RGB gray ramp 0, 1, 2…254, 255, 0, 1, 2…during each active video period
- For each of the TMDS clock and data pairs acting as the tested pair:

- Set the delay for all outputs to 0nS and disable “Differential Timing Offset” if previously enabled.
- Move the TMDS ‘+’ signal of the tested pair to DTG output module A, 1+
- Move the TMDS ‘–‘ signal of the tested pair to DTG output module A, 2+
- Change DTG configuration to output the pattern for the tested TMDS channel on module A, 1
- In the DTG “Timing” screen, select the tested channel (i.e. connected to 1A1). From the “Edit” menu, enable “Differential Timing Offset”.
- Click on the delay value in the Differential Timing Offset column and set to approximately $0.1*T_{BIT}$. This corresponds to the initial intra-pair skew value.
- Increase the skew (Differential Timing Offset) by steps of less than or equal to $0.1*T_{BIT}$, until the Sink DUT outputs errors or until reaching $0.6*T_{BIT}$ or 1nsec.
- If errors seen on DUT:
  - Reduce the skew one step, so that Sink DUT outputs no errors.
  - If intra-pair skew < $0.4*T_{BIT}$, → FAIL.

- Repeat the test for each of the remaining untested pairs.

Test ID 8-7: TMDS – Jitter Tolerance

Reference	Requirement
[HDMI: Table 4-16] Sink AC Characteristics at TP2	TMDS Clock jitter : 0.30 T_{BIT} (relative to Ideal Recovery Clock)
[HDMI: Figure 4-14] Absolute Eye Diagram Mask at TP2 for Sink Requirements	<See reference for details.>

Test Objective

Confirm that the maximum allowed TMDS clock jitter is supported by the Sink DUT.

Required Test Method

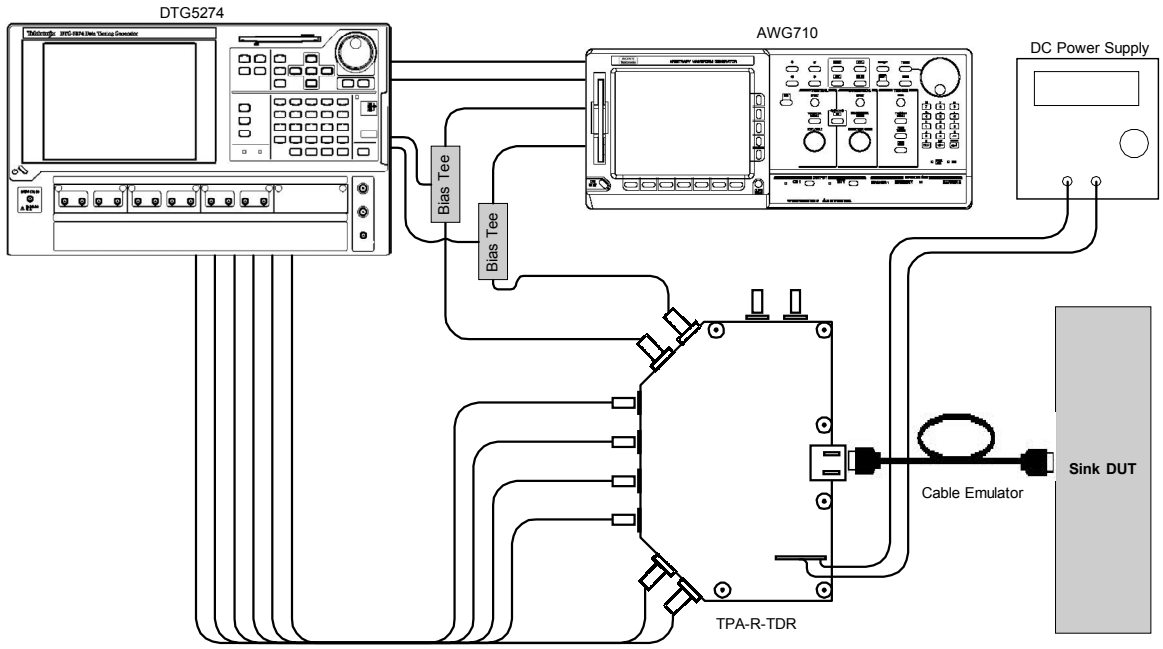
- Operate the Sink DUT to support the HDMI input signal.
- Connect TPA-R to Sink DUT using a Cable Emulator specified for tested pixel clock rate (see below).
- Configure the DTG and AWG as follows:
  - Output any Sink-supported video format that uses the maximum Sink-supported pixel clock rate.
  - No jitter on any output.
- [Determine and use the worst-case TMDS_CLOCK to TMDS_DATA skew condition for the Sink DUT]
  - Set the DTG delay on all channels to this worst-case skew.
- [Measure jitter tolerance while verifying adequate support by Sink (See detail in figure below.)]
  - For each of the two test cases…
    - D_JITTER = 500kHz, C_JITTER = 10MHz
    - D_JITTER = 1MHz, C_JITTER = 7MHz
  - Do the following:
    - Set C_JITTER component to $0.3*T_{BIT}$
    - Increase the D_JITTER component from $0.4*T_{BIT}$ in steps of $0.1*T_{BIT}$ until Sink fails to adequately support signal or until reaching $0.7*T_{BIT}$
    - If maximum supported D_JITTER amplitude < $0.5*T_{BIT}$ → FAIL
    - If maximum supported D_JITTER amplitude < $0.5*T_{BIT}$ → go to VERIFICATION step
    - Set D_JITTER component to $0.5*T_{BIT}$
    - Increase the C_JITTER component from $0.2*T_{BIT}$ in steps of $0.1*T_{BIT}$ until Sink fails to adequately support signal or until reaching $0.5*T_{BIT}$
    - If maximum supported C_JITTER amplitude < $0.25*T_{BIT}$ → FAIL
    - If maximum supported C_JITTER amplitude < $0.3*T_{BIT}$ → go to VERIFICATION step

- If all maximum supported C_JITTER amplitude >= 0.3*T_{BIT} and all maximum supported D_JITTER amplitude >= 0.5*T_{BIT} → PASS

VERIFICATION:

- Measure output eye using method described in Test ID 7-10: TMDS – Data Eye Diagram.
- If output eye has no points within white area shown in Figure 8-1 → FAIL
- If output eye has points within white area → PASS

Recommended Test Method Test ID 8-7: TMDS – Jitter Tolerance



Setup 22. Test ID 8-7: TMDS – Jitter Tolerance

No.	Description	Recommended TE	Reference	Qty.
1	Digital Timing Generator (DTG)	Tektronix DTG5274	4.2.1.2	1
2	Arbitrary Waveform Generator (AWG)	Tektronix AWG710	4.2.1.2	1
3	DC Power Supply	KENWOOD PW18-1.8AQ	4.2.1.14	1
4	SMA Cables	<See reference>	4.2.1.6	12
5	Bias-Tees	Mini-circuits ZFBT-4R2GW	4.2.1.8	2
6	Cable Emulator	<See reference>	4.2.1.16	1
7	TPA-R-TDR	Tektronix TPA-R-TDR	4.2.1.1.7	1

- Operate the Sink DUT to support the HDMI input signal.
- Connect the DTG, AWG, Bias-Tees and TPA-R-TDR as shown above
  - AWG Marker 1+ output to DTG Ext.Clock input
  - AWG Marker 2+ output to DTG Trigger In
  - AWG Ch. 1+ output to Bias-Tee signal input (RF)
    - Bias-Tee signal output to TMDS_CLOCK+ (RF & DC)
    - DTG DC_OUT (1) to Bias-Tee DC-level input (DC)
  - AWG Ch. 1- output to Bias-Tee signal input (RF)
    - Bias-Tee signal output to TMDS_CLOCK- (RF & DC)
    - DTG DC_OUT (2) to Bias-Tee DC-level input (DC)

- DTG Module A, Channel 1+, 1-: No connect
- DTG Module A, Channel 2+, 2-: No connect
- DTG Module B, Channel 1+, 1-: connect to TMDS_DATA0+,-
- DTG Module B, Channel 2+, 2-: connect to TMDS_DATA1+,-
- DTG Module C, Channel 1+, 1-: connect to TMDS_DATA2+,-
- DTG Module C, Channel 2+, 2-: No connect

- Connect TPA-R-TDR to Sink DUT using a Cable Emulator specified for tested pixel clock rate (see below) .
- Connect and configure DC Power Supply to drive +5V between +5V Power (P_5V) and DDC/CEC Ground (P_GND) on TPA-P-TDR.
- Configure the DTG as follows:
  - Output any Sink-supported video format that uses the maximum Sink-supported pixel clock rate.
  - Video data pattern: repeating RGB gray ramp 0, 1, 2…254, 255, 0, 1, 2…during each active video period
  - No jitter on any output.
- Configure AWG as follows:
  - Under “Vertical” menu, set the following:
    - Filter-through
    - Amplitude = 0.5Vpp
    - Offset = 0V
    - Marker 1 = 0.00V to 1.00V
    - Marker 2 = 0.00V to 2.00V
  - No jitter on output initially, with ability to add two simultaneous jitter components.
- [Determine and use the worst-case TMDS_CLOCK to TMDS_DATA skew condition for the Sink DUT, as shown below]
  - For each of the following delay values: $0.0T_{BIT}$, $0.1T_{BIT}$…$1.0T_{BIT}$ do the following:
    - Use the DTG to add the delay to all TMDS_DATA channels.
    - Increase the amplitude of 500kHz jitter (added by the AWG to TMDS_CLOCK) until the Sink fails to adequately support the signal. Record this amplitude.
  - Repeat for remaining delay values, resetting jitter amplitude to 0 before test.
  - The worst-case skew value is located at the point where the lowest amount of jitter is adequately supported by the Sink.
  - Set the DTG delay on all channels to this worst-case skew.
- [Measure jitter tolerance while verifying adequate support by Sink (See detail in figure below.)]
  - For each of the two test cases…
    - D_JITTER = 500kHz, C_JITTER = 10MHz

- D_JITTER = 1MHz, C_JITTER = 7MHz
- Do the following:
  - Set C_JITTER component to 0.3*T_{BIT}
  - Increase the D_JITTER component from 0.4*T_{BIT} in steps of 0.1*T_{BIT} until Sink fails to adequately support signal or until reaching 0.7*T_{BIT}
  - Record maximum supported D_JITTER amplitude (at 0.3*T_{BIT} C_JITTER)
  - If maximum supported D_JITTER amplitude < 0.4*T_{BIT} → FAIL
  - If maximum supported D_JITTER amplitude < 0.5*T_{BIT} → go to VERIFICATION step
  - Set D_JITTER component to 0.5*T_{BIT}
  - Increase the C_JITTER component from 0.2*T_{BIT} in steps of 0.1*T_{BIT} until Sink fails to adequately support signal or until reaching 0.5*T_{BIT}
  - Record maximum supported C_JITTER amplitude (at 0.5*T_{BIT} D_JITTER)
  - If maximum supported C_JITTER amplitude < 0.25*T_{BIT} → FAIL
  - If maximum supported C_JITTER amplitude < 0.3*T_{BIT} → go to VERIFICATION step
- If all maximum supported C_JITTER amplitude >= 0.3*T_{BIT} and all maximum supported D_JITTER amplitude >= 0.5*T_{BIT} → PASS

VERIFICATION:

- With DTG/AWG outputting the failing signal:
- Disconnect Cable Emulator from Sink DUT
- Connect cable to Jitter/Eye Analyzer and measure output eye using method described in Test ID 7-10: TMDS – Data Eye Diagram.
- If output eye has no points within white area shown in Figure 8-1 → FAIL
- If output eye has points within white area → PASS

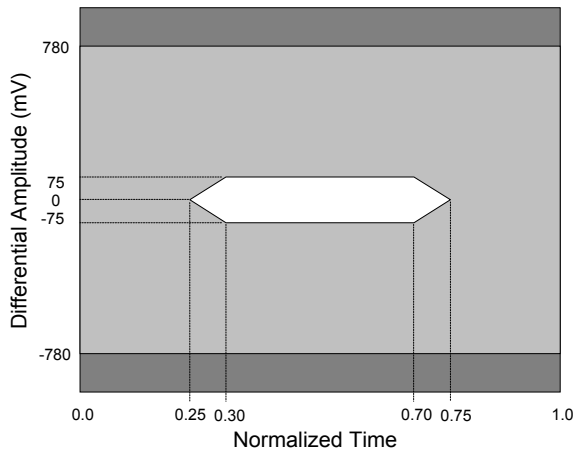
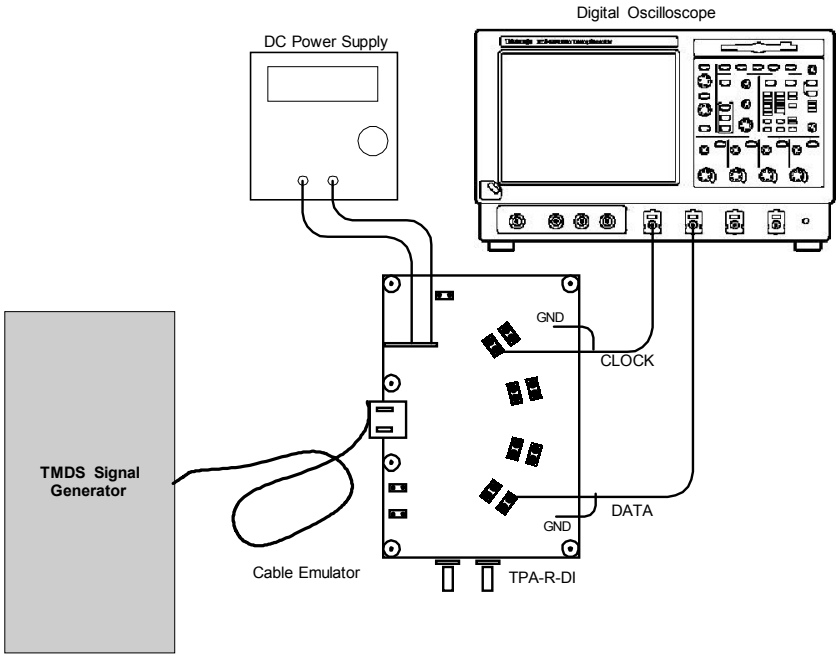
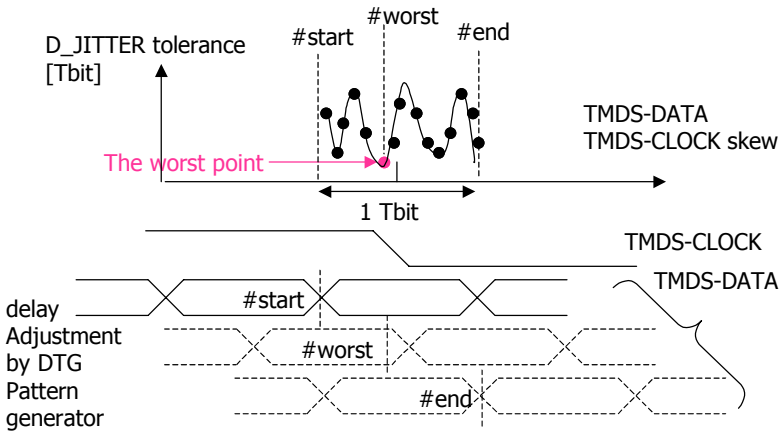


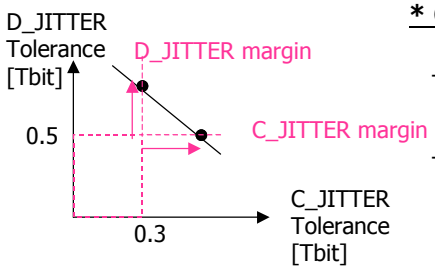
Figure 8-1 Absolute Eye Diagram Mask at TP2 for Sink Requirements


Digital Oscilloscope
DC Power Supply
GND
CLOCK
TMDS Signal Generator
DATA
GND
Cable Emulator
TPA-R-DI

Search for the worst skew point



Jitter margin measurement



*** Conditions**

- Data/Clock skew : worst
  (decided by above method)
- jitter parameter set

AWG
(500kHz, 10MHz)
(1MHz, 7MHz)

Test ID 8-8: TMDS – Differential Impedance

Reference	Requirement
[HDMI: Table 4-17] HDMI Sink Impedance at TP2	Through-connection impedance : 100Ω ± 15% At termination impedance : 100Ω ± 10%

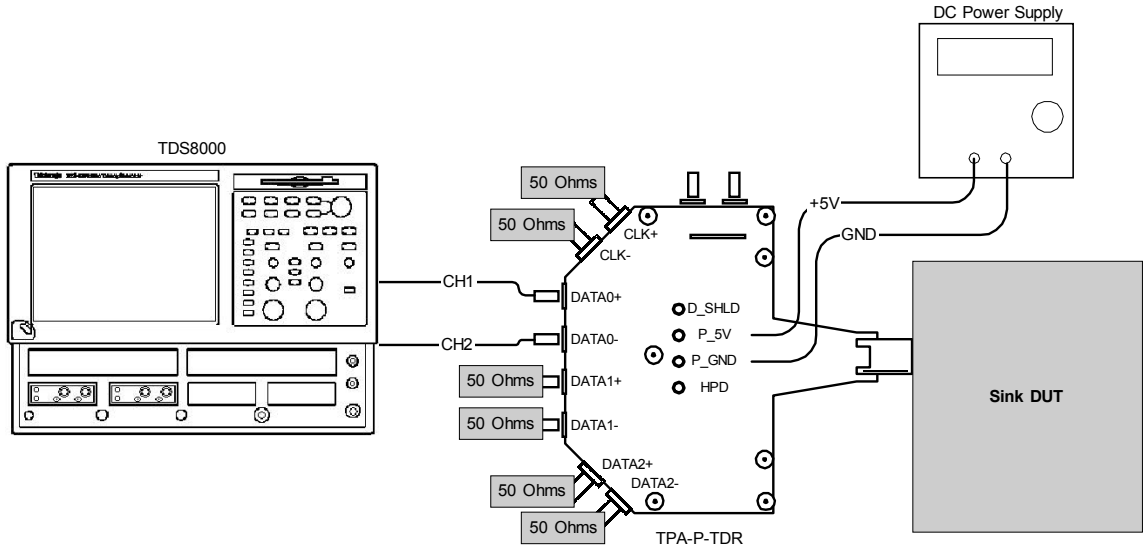
Test Objective

Confirm that the TMDS input impedance of the Sink DUT is within the specified limits.

Required Test Method

- Turn off the power to the Sink DUT.
- Connect the TDR oscilloscope to cables and TPA board but do not connect TPA to the Sink DUT.
- Setup the TDR oscilloscope
- [Determine the measurement distance to DUT input connector]
  - Measure the impedance value along the tested signal path. Note point where impedance hits sharp rise toward high impedance (>200 ohms). This is the distance to the Sink DUT connector.
- Connect the TPA-P-TDR fixture to the Sink DUT HDMI input connector.
- For each of the TMDS clock and data differential pairs:
  - If CDF field Sink_Diff_PowerOn is Y:
    - Measure the impedance value along the tested signal path, from the Sink DUT HDMI input connector to the input pins of the HDMI receiver, Z_{DIFF1}. This is indicated in CDF field Sink_Term_Distance.
    - If (Z_{DIFF_HI} > 115 Ω) OR (Z_{DIFF_LO} < 85 Ω) → FAIL.
  - Else, if CDF field Sink_Diff_PowerOn is N, perform the following:
    - Measure the impedance value (Z_{DIFF2}) along the signal path, from the HDMI input connector until past the termination impedance (where the impedance stabilizes).
    - If (Z_{DIFF_HI} > 115 Ω) OR (Z_{DIFF_LO} < 85 Ω) → FAIL.
- Repeat this measurement for each of the TMDS differential pairs.
- If CDF field Sink_Diff_PowerOn is Y, note that TDR usage under power-on conditions can lead to damage to the TDR oscilloscope. Consequently, the ATC will not perform power on testing.

Recommended Test Method Test ID 8-8: TMDS – Differential Impedance



Setup 23. Test ID 8-8: TMDS – Differential Impedance

No.	Description	Recommended TE	Reference	Qty.
1	TDR/TDT Oscilloscope	Tektronix TDS8000B	4.2.1.10	1
2	DC Power Supply	KENWOOD PW18-1.8AQ	4.2.1.14	1
3	50 Ω SMA Terminators	<See reference>	4.2.1.7	6
4	SMA cables	<See reference>	4.2.1.6	12
5	TPA-P-TDR Fixture	Tektronix TPA-P-TDR	4.2.1.1.6	1

- Turn off the power to the Sink DUT.
- Connect the TPA-P-TDR fixture to the Sink DUT HDMI input connector.
- Setup the TDR/TDT to measure in TDR mode:
  - Normalize each scope channel at the open end of the Test Line, and set a rise time of less than 200ps.
  - Adjust the skew between the two measurement channels to less than 5ps, following the manufacturer's instruction.
  - Set vertical scale to 5 ohms/division, and horizontal scale to 100ps/division.
- Terminate all non-tested TMDS differential pairs with 50 Ω terminators.
- [Determine the measurement distance to DUT input connector]
  - Measure the impedance value along the tested signal path. Note point where impedance hits sharp rise toward high impedance (>200 ohms). This is the distance to the Sink DUT connector.
- Connect the TPA-P-TDR fixture to the Sink DUT HDMI input connector.

- For each of the TMDS clock and data differential pairs:
  - If CDF field Sink_Diff_PowerOn is Y:
    - Measure the impedance value along the tested signal path, from the Sink DUT HDMI input connector to the input pins of the HDMI receiver, Z_{DIFF1}. This is indicated in CDF field Sink_Term_Distance.
    - If (Z_{DIFF_HI} > 115 Ω) OR (Z_{DIFF_LO} < 85 Ω) → FAIL.
  - Else, if CDF field Sink_Diff_PowerOn is N, perform the following:
    - Measure the impedance value (Z_{DIFF2}) along the signal path, from the HDMI input connector until past the termination impedance (where the impedance stabilizes).
    - If (Z_{DIFF_HI} > 115 Ω) OR (Z_{DIFF_LO} < 85 Ω) → FAIL.
- Repeat this measurement for each of the TMDS differential pairs.
- If CDF field Sink_Diff_PowerOn is Y, note that TDR usage under power-on conditions can lead to damage to the TDR oscilloscope. Consequently, the ATC will not perform power on testing.

Test ID 8-9: DDC/CEC Line Capacitance

Reference	Requirement
[HDMI: 4.2.8] DDC	"The Display Data Channel (DDC) I/Os and wires … shall meet the requirements specified in the I^2C Specification, version 2.1, Section 15 for 'Standard Mode' devices."
[HDMI: Table 4-20] Maximum Capacitance of DDC Line	SDA capacitance must be ≤ 50pF at the Sink. SCL capacitance must be ≤ 50pF at the Sink.
[HDMI: Table 4-24] CEC line Electrical Specifications for all Configurations	Maximum capacitance load of a device (excluding cable) 100pF CEC Line Capacitance

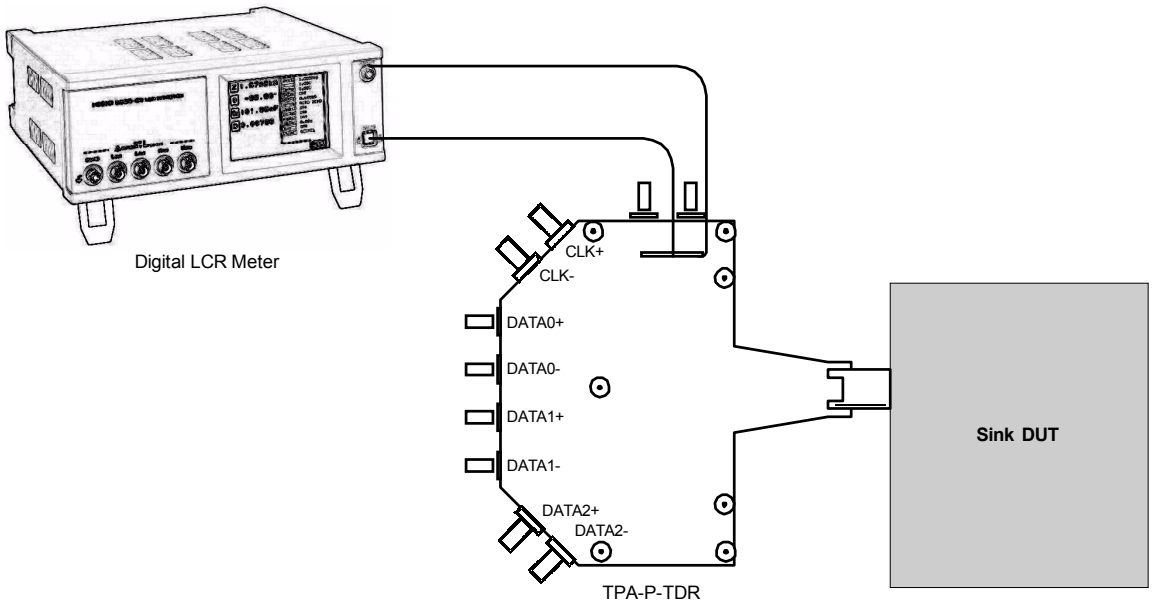
Test Objective

Confirm that the capacitance load on the DDC and CEC lines do not exceed the limit in the specification.

Required Test Method

- Turn off power to the DUT.
- Set LCR meter test signal:
  - Frequency = 100kHz
- Measure C1 as the inherent TPA-P-DI capacitance on the SDA pin.
- Attach TPA-P-DI to DUT and measure capacitance C2 on SDA.
- Net DUT capacitance, C_{DUT} = C2 – C1.
- If C_{DUT} > 50pF, then FAIL.
- Repeat the C1 and C2 measurement for the SCL pin.
- If C_{DUT} > 50pF, then FAIL.
- Set the LCR meter test signal:
  - Frequency = 1kHz
- Repeat the C1 and C2 measurement for the CEC pin.
- If C_{DUT} > 100pF, then FAIL.

Recommended Test Method Test ID 8-9: DDC/CEC Line Capacitance



Setup 24. Test ID 8-9: DDC/CEC Line Capacitance

No.	Description	Recommended TE	Reference	Qty.
1	Digital LCR Meter	HIOKI 3522-50	4.2.1.15	1
2	LCR Meter Probe	HIOKI 9143	4.2.1.15	1
3	TPA-P-TDR Fixture	Tektronix TPA-P-TDR	4.2.1.1.6	1

- Turn off power to the Sink DUT.
- Set LCR meter test signal:
  - Frequency = 100kHz
- Measure C1 as the inherent TPA-P-DI capacitance on the SDA pin.
- Attach TPA-P-DI to Sink DUT and measure capacitance C2 on SDA.
- Net Sink DUT capacitance, C_{SINK} = C2 – C1.
- If C_{SINK} > 50pF, then FAIL.
- Repeat the C1 and C2 measurement for the SCL pin.
- If C_{SINK} > 50pF, then FAIL.
- Set the LCR meter test signal:
  - Frequency = 1kHz
- Repeat the C1 and C2 measurement for the CEC pin.
- If C_{SINK} > 100pF, then FAIL.

Test ID 8-10: HPD Output Voltage

Reference	Requirement
[HDMI: Table 4-22] Required Output Characteristics of Hot Plug Detect Signal	The high voltage level must be within 2.4V to 5.1V. The low voltage level must be within 0.0V to 0.4V. [Note: An errata changing the maximum value to 5.1V will be issued.]

Test Objective

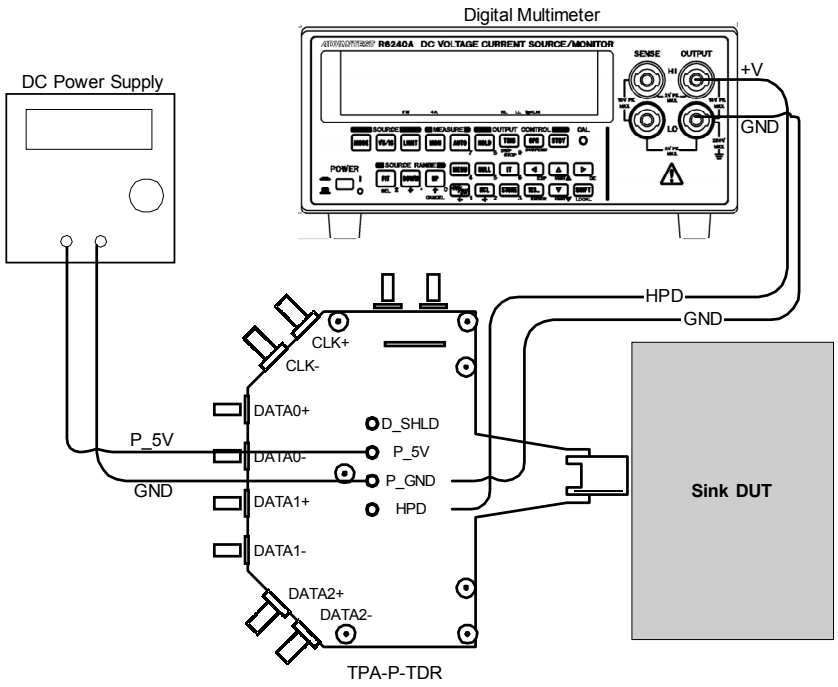
Confirm that the Hot Plug Detect signal returned from the Sink conforms to the specified voltage levels, and that it is not asserted when the +5V Power signal is not asserted.

Required Test Method

- Connect TPA-P-TDR to HDMI input connector of Sink DUT.
- Connect DC power supply to +5V pin on TPA-P-TDR.
- Set the +5V Power pin to 0.0V (= power-off)
  - Measure voltage on the HPD pin of TPA-P-TDR (V_{HPD_L}),
- For +5V Power voltages of 4.8V and 5.1V:
  - Measure voltage on the HPD pin of TPA-P-TDR (V_{HPD_H})
  - If ($0.0 > V_{HPD\_L}$ OR $V_{HPD\_L} > 0.4$) OR ($2.4 > V_{HPD\_H}$ OR $V_{HPD\_H} < 5.1$) → FAIL.

Note: Use 0.1 Volt resolution for the comparison. (i.e. 0.0 means 2 significant digits)

Recommended Test Method Test ID 8-10: HPD Output Voltage



Setup 25. Test ID 8-10: HPD Output Voltage

No.	Description	Recommended TE	Reference	Qty.
1	Digital Multi-Meter	ADVANTEST R6240A	4.2.1.11	1
2	DC Power Supply	KENWOOD PW18-1.8AQ	4.2.1.14	1
3	TPA-P-TDR Fixture	Tektronix TPA-P-TDR	4.2.1.1.6	1

- Connect TPA-P-TDR to HDMI input connector of Sink DUT.
- Connect DC power supply to +5V pin on TPA-P-TDR.
- Set the +5V Power pin to 0.0V (= power-off)
  - Measure voltage on the HPD pin of TPA-P-TDR (V_{HPD_L}),
- For +5V Power voltages of 4.8V and 5.1V:
  - Measure voltage on the HPD pin of TPA-P-TDR (V_{HPD_H})
  - If ($0.0 > V_{HPD\_L}$ OR $V_{HPD\_L} > 0.4$) OR ($2.4 > V_{HPD\_H}$ OR $V_{HPD\_H} < 5.1$) → FAIL.

Note: Use 0.1 Volt resolution for the comparison. (i.e. 0.0 means 2 significant digits)

Test ID 8-11: HPD Output Resistance

Reference	Requirement
[HDMI: Table 4-22] Required Output Characteristics of Hot Plug Detect Signal	The output resistance of the HPD pin must be 1000Ω ±20%.

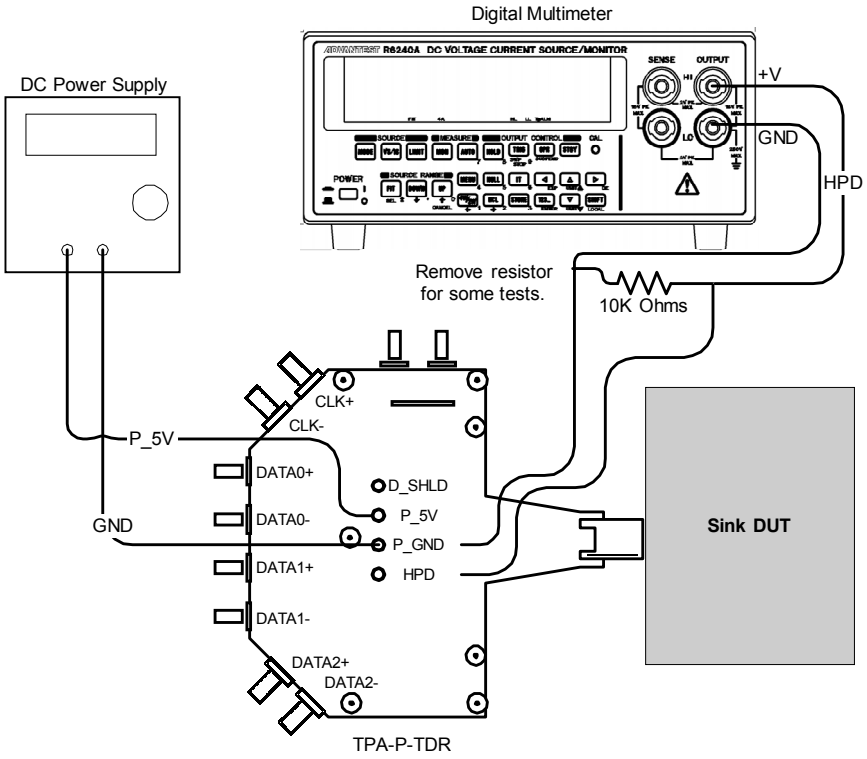
Test Objective

Confirm that the HPD pin on the Sink DUT presents the proper impedance to the source device.

Required Test Method

- Connect TPA-P to Sink DUT.
- Connect and configure DC Power Supply to drive +5V between +5V Power (P_5V) and DDC/CEC Ground (P_GND) on TPA-P-TDR.
- Measure the voltage of the HPD pin on the TPA-P (V_A).
- Connect a 10K Ω resistor between HPD pin and DDC/CEC Ground.
- Measure the HPD pin voltage (V_B).
- Calculate output resistance on HPD pin as:
  - $Z_{HPD} = (V_A/V_B - 1) * 10{,}000$
- If ($Z_{HPD} < 800\Omega$) OR ($Z_{HPD} > 1200\Omega$) → FAIL

Recommended Test Method Test ID 8-11: HPD Output Resistance



Setup 26. Test ID 8-11: HPD Output Resistance

No.	Description	Recommended TE	Reference	Qty.
1	Digital Multi-Meter and Probe	ADVANTEST R6240A	4.2.1.11	1
3	DC Power Supply	KENWOOD PW18-1.8AQ	4.2.1.14	1
3	10K Ω resistor	<any>		
4	TPA-P-TDR Fixture	Tektronix TPA-P-TDR	4.2.1.1.6	1

- Connect TPA-P-TDR to Sink DUT.
- Connect DC Power Supply between +5V Power (P_5V) and DDC/CEC Ground (P_GND) on TPA-P-TDR.
- Set DC Power Supply to output +5.0V.
- Measure the voltage of the HPD pin on the TPA-P-TDR (V_A).
- Connect a 10K Ω resistor between HPD (HOT_PLUG) pin and DDC/CEC Ground (P_GND).
- Measure the HPD pin voltage (V_B).
- Calculate output resistance on HPD pin as:
  - $Z_{HPD} = (V_A/V_B - 1) * 10{,}000$
- If ($Z_{HPD} < 800\Omega$) OR ($Z_{HPD} > 1200\Omega$) → FAIL

Test ID 8-12: +5V Power Max Current

Reference	Requirement
[HDMI: 4.2.7] +5V Power Signal	"A Sink shall not draw more than 50mA of current from the +5V Power pin. When the Sink is powered on, it can draw no more than 10mA from the +5V Power signal."

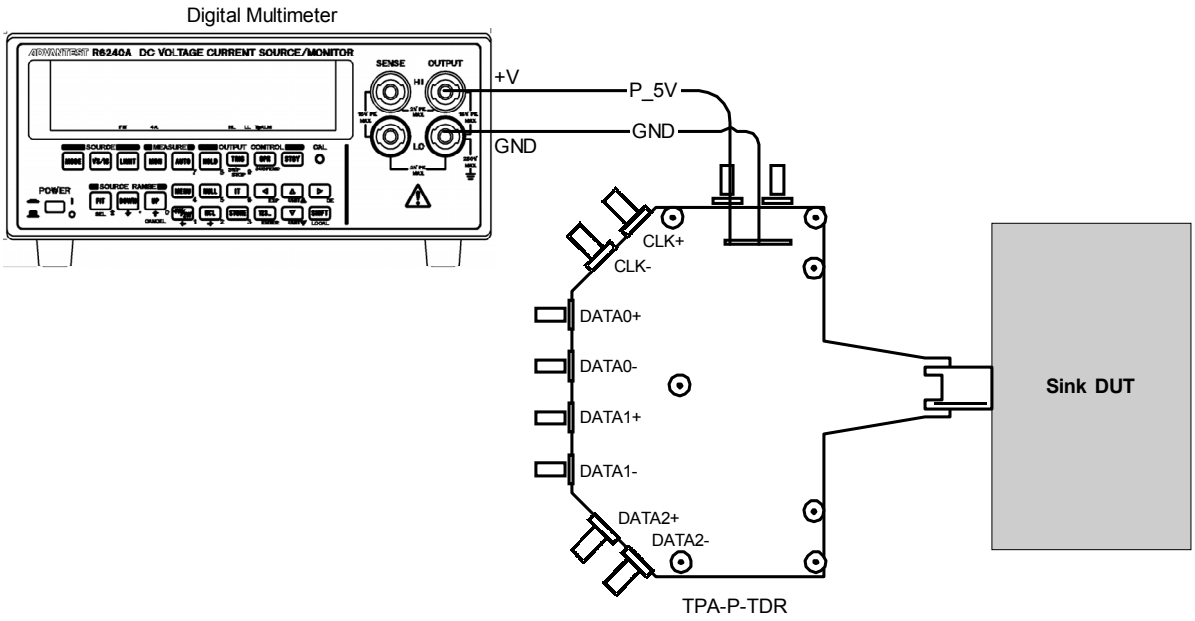
Test Objective

Confirm that the Sink DUT does not consume more power than allowed when in either the ON or OFF state, from the +5V Power pin.

Required Test Method

- Connect TPA-P to HDMI input connector of Sink DUT.
- For the three cases, Sink DUT powered ON, Sink DUT powered OFF, and Sink DUT disconnected from AC power source, do the following:
- Set current limit of power supply to 65mA
- For the two voltages at the +5V pin of 4.9V and 5.1V, do the following:
  - Measure the current drawn through the +5V Power pin by the Sink, I_{SINK}
  - If (Sink DUT power is ON) AND ($I_{SINK} \geq 10mA$) then FAIL.
  - If (Sink DUT power is OFF or disconnected from AC) AND ($I_{SINK} \geq 50mA$) then FAIL.

Recommended Test Method Test ID 8-12: +5V Power Max Current



Setup 27. Test ID 8-12: +5V Power Max Current

No.	Description	Recommended TE	Reference	Qty.
1	DC Power Supply	KENWOOD PW18-1.8AQ	4.2.1.14	1
2	TPA-P-TDR Fixture	Tektronix TPA-P-TDR	4.2.1.1.6	1

Note: The following current measurements may be made using an accurate current meter built into the Power Supply, if available.

- Connect TPA-P-TDR to HDMI input connector of Sink DUT.
- For the three cases, Sink DUT powered ON, Sink DUT powered OFF, and Sink DUT disconnected from AC power source, do the following:
- Set current limit of power supply to 65mA
- For the two voltages at the +5V pin of 4.9V and 5.1V, do the following:
  - Measure the current drawn through the +5V Power pin by the Sink, I_{SINK}
  - If (Sink DUT power is ON) AND ($I_{SINK} \geq$ 10mA) then FAIL.
  - If (Sink DUT power is OFF or disconnected from AC) AND ($I_{SINK} \geq$ 50mA) then FAIL.

Test ID 8-13: CEC Line Connectivity

NOTE: This test only needs to be performed once per product, not once per connector as with all of the other tests in this document.

Reference	Requirement
[HDMI: Table 4-24] CEC Line Connectivity	<See reference for details>

Test Objective

If the DUT has more than one input connection ensure that any input connections and output connections are connect as specified in following description:

CEC lines from all HDMI inputs (if present) and a single HDMI output (if present) shall be interconnected.

Except :

- A device which has no HDMI output is allowed to have separate CEC lines for each HDMI connector if that device takes a logical address of 0 on each CEC line.
- A TV that is acting as the root shall not connect the CEC line to any HDMI output.

Required Test Procedure

- Turn DUT off
- If CDF field CDF_HDMI_output_count == 0 then:
  - For every combination of HDMI connectors on the DUT measure the resistance between the CEC connection of each. If each resistance measurement is less than 2Ω or greater than 48KΩ then PASS else FAIL.
- else
  - If CDF field Sink_Display == Y then:
    - For every combination of HDMI input connectors on the DUT measure the resistance between the CEC connections of each. If any resistance measurement is in range 2Ω < R < 48KΩ then FAIL
    - For every output connection measure the resistance between its CEC connections of it and each input connection. If any resistance measurement is in less than 1MΩ then FAIL else PASS.
  - Else:
    - For every combination of HDMI input connectors on the DUT measure the resistance between the CEC connections of each. If any resistance measurement > 2Ω then FAIL
    - For every output connection measure the resistance between the CEC connections of it and each input connection. If any resistance measurement is in less than 1MΩ then note the output connection ID.

- If more than one output connection ID noted then FAIL (as product has CEC line connected to > 1 output)
- Choose any input connector on the DUT measure the resistance between the CEC connection of this input and the CEC connection of the noted output connection. If resistance measurement > 2Ω then FAIL else PASS.

Recommended Test Method

No.	Description	Recommended TE	Reference	Qty.
1	Digital Multi-Meter	ADVANTEST R6240A	4.2.1.11	1
2	TPA-P-SE	Tektronix TPA-P-SE	4.2.1.1.4	1
3	TPA-P-DI	Tektronix TPA-P-DI	4.2.1.1.2	1

- Turn DUT off
- Set Digital Multi-Meter to measure resistance using auto scale mode.
- If CDF field CDF_HDMI_output_count == 0:
  - For every combination of HDMI connectors on the DUT
    - Connect TPA-P to each selected HDMI connector
    - Connect the meter to the CEC connection on each TPA-P
    - Read resistance value from Digital Multi-Meter
    - If reading is less than 2Ω or greater than 48KΩ → PASS, else FAIL
- else:
  - If CDF field Sink_Display == Y then:
    - For every combination of HDMI input connectors on the DUT
      - Connect TPA-P to each selected HDMI connector
      - Connect the meter to the CEC connection on each TPA-P
      - Read resistance value from Digital Multi-Meter
      - If reading is less than 2Ω or greater than 48KΩ → PASS and continue else FAIL
    - For every output connection:
      - Connect TPA-P to each selected HDMI connector
      - Connect the meter to the CEC connection on each TPA-P
      - Read resistance value from Digital Multi-Meter
      - If reading is less than 48KΩ → FAIL
  - Else (CDF field Sink_Display == N)
    - For every combination of HDMI input connectors on the DUT
      - Connect TPA-P to each selected HDMI connector
      - Connect the meter to the CEC connection on each TPA-P

- Read resistance value from Digital Multi-Meter
- If reading is greater than 2Ω → FAIL

- For every output connection:
  - Connect TPA-P to each selected HDMI connector
  - Connect the meter to the CEC connection on each TPA-P
  - Read resistance value from Digital Multi-Meter
  - If reading is less than 48KΩ then note the output connection ID
- If more than one output connection ID noted → FAIL (as product has CEC line connected to > 1 output)
- If no output connection ID noted → FAIL (as product does not connect CEC line to any output)
- Choose any input connector on the DUT connect TPA-P to it,connect the Digital Multi-Meter to its CEC connection
- Connect TPA-P to noted output connection and Digital Multi-Meter Probe to its CEC connection
- Read resistance value from Digital Multi-Meter
- If reading is >2Ω → FAIL else PASS

Test ID 8-14: CEC Line Degradation

NOTE: This test only needs to be performed once per product, not once per connector as with all of the other tests in this document.

Reference	Requirement
[HDMI: Table 4-24] Power off characteristics	<See reference for details>

Test Objective

Ensure that the DUT does not degrade communication between other CEC devices when power is applied, when power is removed and, if supported, in standby mode (the line must not be pulled down by the powered off device).

Required Test Procedure

- Measure CEC line voltage on DUT, V_{CEC1}, if voltage 0v or 3.3v ±10% then continue else → FAIL
- Connect the CEC line on DUT to 3.3v via a 27Kohm ±5% resistor
- Measure CEC line voltage if voltage not 3.3v ±10% then → FAIL
- Connect the CEC line on the DUT input connector to DDC/CEC Ground via 1k ohm ±5% load resistor (as well as the previously connected 3.3v via 27KΩ)
- Measure CEC line voltage on the DUT output connector, V_{CEC2}
- If V_{CEC1} = 0v and V_{CEC2} not in range 0.12v ±12% then → FAIL
- If V_{CEC1} = 3.3v ±10% and V_{CEC2} not 0.24v ±12% then → FAIL
- Repeat tests in power off state
- If standby power mode exists on DUT, repeat test in that state

Recommended Test Method

No.	Description	Recommended TE	Reference	Qty.
1	Digital Multi-Meter	ADVANTEST R6240A	4.2.1.11	1
3	27KΩ ±5% resistor	<any>		1
3	1KΩ±5% Resistor	<any>		1
4	TPA-P-SE	Tektronix TPA-P-SE	4.2.1.1.4	1

- Power on DUT
- Connect TPA to DUT
- Set DC Power Supply to 3.3V
- Set Multi-Meter to voltage measurement and connect between CEC pin and DDC/CEC Ground on TPA

- Measure voltage with multi-Meter, record as V_{CEC1}
- if V_{CEC1} 0v or 3.3v ±10% then continue else → FAIL
- Connect the CEC line on TPA to DC Power Supply via the 27Kohm ±5% resistor
- Measure voltage if voltage not 3.3v ±10% then → FAIL
- Connect the CEC line on the TPA input connector to DDC/CEC Ground on TPA via 1k ohm ±5% load resistor (as well as the previously connected 3.3v via 27KΩ)
- Measure voltage, record as V_{CEC2}
- If V_{CEC1} = 0v and V_{CEC2} not in range 0.12v ±12% then → FAIL
- If V_{CEC1} = 3.3v ±10% and V_{CEC2} not 0.24v ±12% then → FAIL
- Repeat tests in power off state
- If standby power mode exists on DUT, repeat test in that state

8.4 Sink – Protocol

The Sink DUT must be turned on and configured to accept signals via the HDMI input. Some mechanism must be in place to determine if Sink DUT is adequately supporting the transmitted audio and video signals.

The conditions in the following tests will be generated by the TE to verify the Sink DUT's support. The Sink must continually support the transmitted signal during the entire sequence of test conditions.

Test ID 8-15: Character Synchronization

Reference	Requirement
[HDMI: 5.2.1.2] Character Synchronization	The Sink is required to establish synchronization with the data stream during any Control Period greater than or equal to $t_{S,min}$ (12) characters in length.

Test Objective

Verify that the Sink establishes synchronization with the data when it receives only minimum-length Control Periods.

Required Test Method

- Connect the Sink DUT to a TMDS Protocol Generator
- Begins with no TMDS clock for 2 seconds.
- Protocol Generator starts transmission of valid 640x480p video frame with every horizontal and vertical blanking interval completely filled with one or more Data Islands and with all Control Periods either 12 or 13 characters in length. Note: 640x480p has 158 pixels in HBLANK low. Best arrangement is: 13+2+32+32+32+32+2+13 = 158. There are 7200 pixels in VBLANK so multiple arrangements may be possible..
- If Sink DUT does not support the transmitted video and audio format → FAIL

Recommended Test Method

- Connect TPA-P to HDMI input connector of Sink DUT.
- Connect TMDS Protocol Generator to all TMDS differential pairs.
- Configure the TMDS Protocol Generator (Tektronix DTG527) to output above required test signal pattern.
- If Sink adequately supports signal → PASS, else → FAIL

Test ID 8-16: Acceptance of All Valid Packet Types

Reference	Requirement
[HDMI: 5.3] Data Island Packet Definition	"Sink shall support reception of any valid packet type."

Test Objective

Verify that Sink supports reception of all valid packet types.

Required Test Method

- TE transmits 720x480p or 720x576p (depending upon 60Hz/50Hz capability), 2 channel 48kHz audio HDMI signal with following characteristics:
- During VBLANK, one or more Data Islands containing a valid
  - Null Packet (0x00)
  - General Control Packet (0x03)
  - Vendor-specific InfoFrame Packet (0x81)
  - AVI InfoFrame Packet (0x82)
  - Source Product Description Packet (0x83)
  - Audio InfoFrame Packet (0x84)
  - MPEG Source InfoFrame Packet (0x85).
- The Vendor-specific InfoFrame Packet will contain a length of 3 and a 24-bit IEEE registration identifier belonging to the HDMI Licensing, LLC (0x000C03).
- The General Control Packet will have Set_AVMUTE and Clear_AVMUTE clear (0).
- If Sink DUT does not adequately support the signal → FAIL

Recommended Test Method

- Connect TPA-P to HDMI input connector of Sink DUT.
- Connect TMDS Protocol Generator to all TMDS differential pairs.
- Configure the TMDS Protocol Generator (Tektronix DTG527) to output above required Test signal pattern..
- If Sink adequately supports signal → PASS, else → FAIL

8.5 Sink – Video

Test ID 8-17: 861B Format Support Requirements

Reference	Requirement
[861B: 7.2.2] Full 861B Implementation	If an EIA/CEA-861B-defined video format is supported by the Sink, it shall be indicated in an SVD and optionally, by a DTD.
	All 240 and 480 line 861B-defined formats described in DTD shall be listed as 59.94Hz.
	All 720 and 1080 line 861B-defined formats described in DTD, near 59.94/60Hz shall be listed as 60Hz.
	"The required 861/861A formats shall…be advertised using the EDID 18-byte Detailed Timing Descriptors (for backward compatibility)."

Test Objective

Verify that no 861B-defined video format is declared only in a Detailed Timing Descriptor.

Required Test Method

Note that aspect ratios (AR) for Detailed Timing Descriptors are calculated as:

ar = Horizontal / Vertical

if 1.2667 < ar < 1.04 → AR = 4:3 [1.33 ± 5%]

else if 1.6889 < ar < 1.8667 → AR = 16:9 [1.78 ± 5%]

else, AR = unknown.

- [If an EIA/CEA-861B-defined video format is supported by the Sink, it shall be indicated by an SVD and optionally, by a DTD.]
  - For each DTD in EDID:
    - Examine DTD for match with any 861B-defined formats. Such a DTD will have:
      - All fields in the DTD for horizontal and vertical active and total are equal to the values shown in EIA/CEA-861B Table 4, for a specific format.
      - Pixel clock frequency in bytes 0 and 1 within ±1% of 861B-specified frequency for the format.
      - Aspect ratio (calculated as H/V) within ±5% of either 16:9 or 4:3.
    - If DTD matches any 861B format, search SVDs for that same video format at same aspect ratio.
    - If no matching SVD → FAIL
    - If DTD matches one of the following…

- Format 1: 640x480p @ 59.94/60Hz, pixel clock 25.175MHz [=0x09D6]
- Format 2 or 3: 720x480p @ 59.94/60Hz, pixel clock 27.00MHz [=0x0A8C]
- Format 14 or 15: 1440x480p @ 59.94/60Hz, pixel clock 54.00MHz [=0x1518]
- Format 6 or 7: 1440x480i @ 59.94/60Hz, 27.00MHz
- Format 10 or 11: 2880x480i @ 59.94/60Hz, 54.00MHz
- Format 8 or 9: 1440x240p @ 59.94/60Hz, 27.00MHz
- Format 12 or 13: 2880x240p @ 59.94/60Hz, 54.00MHz
- Format 4: 1280x720p @ 59.94/60Hz, pixel clock 74.25MHz [=0x1D01]
- Format 5: 1920x1080i @ 59.94/60Hz, 74.25MHz
- Format 16: 1920x1080p @ 59.94/60Hz, 148.5MHz [=0x3A02]

- …then pixel clock frequency of DTD shall be exactly value shown above.
- If pixel clock frequency of DTD does not exactly match → FAIL

- ["The required 861/861A formats shall…be advertised using the EDID 18-byte Detailed Timing Descriptors (for backward compatibility)."]
  - For each SVD in EDID:
    - If SVD matches one of the following…
      - 720x480p @ 59.94/60Hz
      - 1280x720p @ 59.94/60Hz
      - 1920x1080i @ 59.94/60Hz
      - 720x576p @ 50Hz
      - 1280x720p @ 50Hz
      - 1920x1080i @ 50Hz
    - …then search for DTD matching (per algorithm above) the format at the same aspect ratio.
    - If no corresponding DTD found → FAIL
- [861B: 7.2.2] First DTD in EDID Block 0 shall be the "preferred" video format and shall have the primary AR of Sink.
  - Examine first DTD in EDID Block 0 for aspect ratio. Examine CDF field Sink_PrimaryAR (primary aspect ratio of display).
  - If aspect ratios do not match → FAIL

Recommended Test Method

- If the EDID image has not yet been captured from the Sink:
  - Connect Sink DUT to Silicon Image EDID Reader/Analyzer. Run EDID Analysis software and execute command "Read from DDC", followed by "Save As…". Save file in an appropriate location.
  - If any errors are reported during EDID read → FAIL (DDC read).
- Launch EDID Analysis tool and open the EDID image.

- Execute EDID Analysis command “HDMI Analysis”.
- If any errors are reported → FAIL, <error comment>
- Perform steps in Required Test Method against viewed EDID image
- PASS/FAIL criteria defined above

Test ID 8-18: HDMI Format Support Requirements

Reference	Requirement
[HDMI: 6.2.1] [Video] Format Support Requirements	"An HDMI Sink which accepts 60Hz video formats shall support the 640x480p @ 59.94/60Hz and 720x480p @ 59.94/60Hz video format timings." "An HDMI Sink which accepts 60Hz video formats, and which supports HDTV capability, shall support 1280x720p @ 59.94/60Hz or 1920x1080i @ 59.94/60Hz video format timings." "An HDMI Sink which accepts 50Hz video formats shall support the 640x480p @ 59.94/60Hz and 720x576p @ 50Hz video format timings." "An HDMI Sink which accepts 50Hz video formats, and which supports HDTV capability, shall support 1280x720p @ 50Hz or 1920x1080i @ 50Hz video format timings." "An HDMI Sink that is capable of receiving any of the following video format timings using any other component analog or uncompressed digital video input, shall be capable of receiving that format across the HDMI interface.1280x720p @ 59.94/60Hz, 1920x1080i @ 59.94/60Hz, 1280x720p @ 50Hz, 1920x1080i @ 50Hz"
[861B: Annex A] Example EDID 18-Byte Detailed Timing Descriptors	<See reference for details.>

Test Objective

Verify that Sink DUT indicates support for all required Video Formats in its EDID.

Required Test Method

Note that the following steps simply examine the EDID for indicated support of the required formats.

Perform the following:

- If the CDF field Sink_60Hz is 'Y', then perform the following:
  - Examine EDID for an SVD containing video format code 2 or 3.
  - If no SVD contains 2 or 3 → FAIL
  - If the CDF field Sink_HDTV is 'Y', then perform the following:
    - Examine EDID for an SVD containing video format code 4 or 5.
    - If no SVD contains 4 or 5 → FAIL
- If the CDF field Sink_50Hz is 'Y', then perform the following:
  - Examine EDID for SVD containing video format code 17 or 18 (720x576p @ 50Hz).
  - If no SVD contains 17 or 18 → FAIL

- If the CDF field Sink_HDTV is “Y”, then perform the following:
  - Examine EDID for an SVD containing video format code 19 or 20.
  - If no SVD contains 19 or 20 → FAIL
- [Tested Format: 1280x720p @ 59.94/60Hz]

If CDF field

Field Name	*Field Definition*	*Choices*	*Repeater Mini-CDF*
Sink_720p60	Tested Format : 1280x720p @ 59.94/60Hz Is DUT capable of supporting Tested Format using any other component analog or uncompressed digital video output?	Y/N	N

  - == 'Y' then:
    - If no SVD contains 4 → FAIL
- [Tested Format: 1920x1080i @ 59.94/60Hz]
  - If CDF field Sink_1080i60 == 'Y' then:
    - If no SVD contains 5 → FAIL
- [Tested Format: 1280x720p @ 50Hz]
  - If CDF field Sink_720p50 == 'Y' then:
    - If no SVD contains 19 → FAIL
- [Tested Format: 1920x1080i @ 50Hz]
  - If CDF field Sink_1080i50 == 'Y' then:
    - If no SVD contains 20 → FAIL

Recommended Test Method

- If the EDID image has not yet been captured from the Sink:
  - Connect Sink DUT to Silicon Image EDID Reader/Analyzer. Run EDID Analysis software and execute command "Read from DDC", followed by "Save As…". Save file in an appropriate location.
  - If any errors are reported during EDID read → FAIL (DDC read).
- Launch EDID Analysis tool and open the EDID image.
- Execute EDID Analysis command "HDMI Analysis".
- If any errors are reported → FAIL, <error comment>
- Perform steps in Required Test Method against viewed EDID image
- PASS/FAIL criteria defined above

Test ID 8-19: Pixel Encoding Requirements

Reference	Requirement
HDMI: 6.2.3] Pixel Encoding Requirements	"All HDMI Sinks shall be capable of supporting both YC_BC_R 4:4:4 and YC_BC_R 4:2:2 pixel encoding when that device is capable of supporting a color-difference color space from any other component analog or digital video input." "If an HDMI Sink supports either YC_BC_R 4:2:2 or YC_BC_R 4:4:4 then both shall be supported."
[HDMI: 8.3.4] Audio and Video Details	"A Sink may indicate support for YC_BC_R pixel encodings. To indicate support, bits 4 and 5 of byte 3 of the EDID Timing Extension shall both be set to one (see Table 29 of EIA/CEA-861B). To indicate no support, bits 4 and 5 shall both be zero."

Test Objective

Verify that Sink supports YC_BC_R pixel encoding when required.

Required Test Method

- [If an HDMI Sink supports either YC_BC_R 4:2:2 or YC_BC_R 4:4:4 then both shall be supported.]
  - Check bits #4 and #5 of byte #3 of the CEA EDID Timing Extension. [861B: Table 29]
  - If bit # 4 == 1 and bit #5 == 0 → FAIL
  - If bit # 4 == 0 and bit #5 == 1 → FAIL
- [All HDMI Sinks shall be capable of supporting both YC_BC_R 4:4:4 and YC_BC_R 4:2:2 pixel encoding when that device is capable of supporting a color-difference color space from any other component analog or digital video input.]
  - If CDF field Sink_YUV_On_Other == 'Y':
    - Check bits #4 and #5 of byte #3 of the EDID Timing Extension.
    - If either bit clear (0) → FAIL
- [All HDMI Sinks shall be capable of supporting RGB 4:4:4 pixel encoding.]
  - Transmit HDMI video signal with RGB pixel encoding to Sink DUT.
  - If Sink DUT does not adequately support transmitted video → FAIL
- [If bits #4 or #5 of byte #3 of the EDID Timing Extension are set to one then Sink shall be capable of supporting a YC_BC_R pixel-encoded signal.]
  - Transmit a 720x480p or 720x576p (depending upon 60Hz/50Hz capability) signal to Sink DUT using YC_BC_R 4:2:2 pixel-encoding.
  - If DUT does not adequately support transmitted video → FAIL
  - Transmit a 720x480p or 720x576p (depending upon 60Hz/50Hz capability) signal to Sink DUT using YC_BC_R 4:4:4 pixel-encoding.
  - If DUT does not adequately support transmitted video → FAIL

Recommended Test Method

- If the EDID image has not yet been captured from the Sink:
  - Connect Sink DUT to Silicon Image EDID Reader/Analyzer. Run EDID Analysis software and execute command “Read from DDC”, followed by “Save As…”. Save file in an appropriate location.
  - If any errors are reported during EDID read → FAIL (DDC read).
- Launch EDID Analysis tool and open the EDID image.
- Execute EDID Analysis command “HDMI Analysis”.
- If any errors are reported → FAIL
- For EDID based tests perform steps in Required Test Method against viewed EDID image
- PASS/FAIL criteria defined above

- Connect Sink DUT to Audio/Video Protocol Generator
- Transmit HDMI video signal with RGB pixel encoding to Sink DUT.
- If Sink DUT does not adequately support transmitted video → FAIL
- If bits #4 or #5 of byte #3 of the EDID Timing Extension are set to one then:
  - Transmit a 720x480p or 720x576p (depending upon 60Hz/50Hz capability) signal to Sink DUT using YC_BC_R 4:2:2 pixel-encoding.
  - If Sink DUT does not adequately support the transmitted video → FAIL
  - Transmit a 720x480p or 720x576p (depending upon 60Hz/50Hz capability) signal to Sink DUT using YC_BC_R 4:4:4 pixel-encoding.
  - If Sink DUT does not adequately support the transmitted video → FAIL

Test ID 8-20: Video Format Timing

Reference	Requirement
[861B: 4] Video Formats and Waveform Timings	<See reference for details.>

Test Objective

Verify that Sink supports required variations on mandatory video formats and EIA/CEA-861B video formats indicated in EDID.

Required Test Method

Connect the Audio/Video Protocol Generator to the Sink DUT.

For each tested format and pixel clock frequency, configure the Audio/Video Protocol Generator to generate a test pattern in the given format at the tested pixel clock frequency. The test pattern should permit the operator to determine if the Sink displays the image with no significant distortions (spurious dots, horizontal or vertical jitter, incorrect colors) and in the expected aspect ratio and position.

All EIA/CEA-861B-defined video formats listed in the EDID shall be tested at two different pixel clock frequencies. The two different frequencies shall be the minimum and maximum permitted by a Source. For 50Hz formats, these values are 49.75Hz and 50.25Hz (50Hz ± 0.5%). For 59.94Hz or 60Hz formats, these frequencies are 59.64Hz (59.94Hz – 0.5%) and 60.3Hz (60Hz + 0.5%). The tested pixel clock frequency accuracy shall be ±0.05%.

It is permitted for the ATC to not test formats listed in [HDMI: 6.3.2] as “Optional Video Formats”.

- [Verify that Sink DUT supports 640x480p.]
  - Configure the Audio/Video Protocol Generator to transmit 640x480p @ 60Hz to the Sink DUT at the minimum allowable pixel clock frequency.
  - If the Sink DUT does not adequately support format → FAIL, “640x480p, Max”
  - Configure Audio/Video Protocol Generator to transmit 640x480p @ 60Hz to Sink DUT at the maximum allowable pixel clock frequency.
  - If the Sink DUT does not adequately support format → FAIL, “640x480p, Min”
  - If EDID Established Timings has the “640x480p @ 60Hz” bit set
    - If Sink DUT does not adequately support format as underscan, roughly-centered and near-full-screen → FAIL
- For each video format listed in an SVD:
  - [An HDMI Sink DUT which indicates support for EIA/CEA-861B Format 8 or 9 (1440x240p), shall support both variations of the format (22 and 23 vertical blanking lines).]
  - If tested SVD indicates video formats 8 or 9:
    - For each of the timing variations on the 1440x240p @ 59.94Hz video format:

        - Configure the Audio/Video Protocol Generator to transmit the timing variation to the Sink DUT at the minimum allowable pixel clock frequency.
        - If the Sink DUT does not adequately support format → FAIL
        - Configure the Audio/Video Protocol Generator to transmit the timing variation to the Sink DUT at the maximum allowable pixel clock frequency.
        - If the Sink DUT does not adequately support format → FAIL
- [An HDMI Sink DUT which indicates support for EIA/CEA-861B Format 12 or 13 (2880x240p) shall support both variations of this format (22 and 23 vertical blanking lines).]
- If tested SVD indicates video formats 12 or 13:
    - For each of the timing variations on the 2880x240p @ 59.94Hz video format:
        - Configure the Audio/Video Protocol Generator to transmit the timing variation to the Sink DUT at the minimum allowable pixel clock frequency.
        - If the Sink DUT does not adequately support format → FAIL
        - Configure the Audio/Video Protocol Generator to transmit the timing variation to the Sink DUT at the maximum allowable pixel clock frequency.
        - If the Sink DUT does not adequately support format → FAIL
- [An HDMI Sink DUT which indicates support for EIA/CEA-861B Format 23 or 24 (1440x288p) shall support all variations of this format (24, 25 and 26 vertical blanking lines).]
- If tested SVD indicates video formats 23 or 24:
    - For each of the timing variations on the 1440x288p @ 50Hz video format:
        - Configure the Audio/Video Protocol Generator to transmit the timing variation to the Sink DUT at the minimum allowable pixel clock frequency.
        - If the Sink DUT does not adequately support format → FAIL
        - Configure the Audio/Video Protocol Generator to transmit the timing variation to the Sink DUT at the maximum allowable pixel clock frequency.
        - If the Sink DUT does not adequately support format → FAIL
- [An HDMI Sink DUT which indicates support for EIA/CEA-861B Format 27 or 28 (2880x288p) shall support all variations of this format (24, 25 and 26 vertical blanking lines).]
- If tested SVD indicates video formats 27 or 28:
    - For each of the timing variations on the 2880x288p @ 50Hz video format:
        - Configure the Audio/Video Protocol Generator to transmit the timing variation to the Sink DUT at the minimum allowable pixel clock frequency.
        - If the Sink DUT does not adequately support format → FAIL
        - Configure the Audio/Video Protocol Generator to transmit the timing variation to the Sink DUT at the maximum allowable pixel clock frequency.
        - If the Sink DUT does not adequately support format → FAIL
- If tested SVD indicates any format other than 8, 9, 12, 13, 23, 24, 27, or 28, perform the following tests:

- Configure Audio/Video Protocol Generator to transmit that video format to Sink DUT at the minimum allowable pixel clock frequency.
  - If the Sink DUT does not adequately support format → FAIL
- Configure Audio/Video Protocol Generator to transmit that video format to Sink DUT at the maximum allowable pixel clock frequency.
  - If the Sink DUT does not adequately support format → FAIL

Recommended Test Method

Perform Required Test Sequence above using either of the Recommended Audio/Video Protocol Generators.

PASS/FAIL criteria given above.

8.6 Sink – Audio

8.6.1 Audio Test A/V Formats

All tests listed in the following section shall use the following combination of video and audio formats.

- Mandatory video format and audio format with the highest audio sample packet rate available
- Any Video format with lowest line frequency and audio format with the highest audio sample packet rate available
- Audio format with highest audio sample rate available for the product using whatever video format is required to carry that audio format.

The video pattern may be any pattern that can show that the Sink DUT is functioning.

The audio pattern will be a sine wave signal at a frequency of 1kHz with amplitude of –20dBs unless an alternate is specified by the test.

8.6.2 Tests

Test ID 8-21: Audio Clock Regeneration

Reference	Requirement
[HDMI: 7.2] Audio Sample Clock Capture and Regeneration	<See reference for details.>

Test Objective

Verify proper Sink operation with respect to Audio Clock Regeneration.

Required Test Method

For each of the A/V formats described in 8.6.1 above:

- [Verify audio clock regeneration using minimum N parameter.]
  - Transmit ACR packets data with minimum N parameter which is minimum integer value no less than 128*Fs / 1500 and audio sample. A sine wave signal at a frequency of 1kHz with amplitude of –20dBs as the audio test signal should be used. Check produced sound with speakers.
  - Perform listening test
  - If no sound, extraneous sound (e.g. clacking sound), or unnecessary mute (e.g. short term mute, etc) → FAIL
- [Verify audio clock regeneration using maximum N parameter.]
  - Transmit ACR packets with maximum N parameter which is maximum integer value no more than 128*Fs / 300 and audio sample data. A sine wave signal at a frequency of 1kHz with amplitude of –20dBs as the audio test signal should be used.
  - Perform listening test
  - If no sound, extraneous sound (e.g. clacking sound), or unnecessary mute (e.g. short term mute, etc) → FAIL

Recommended Test Method

- Connect TPA-P-TDR to HDMI input connector of Sink DUT.
- Connect Tektronix DTG5274 to all TMDS differential pairs on the TPA-P-TDR.
- Configure the Tektronix DTG5274 to output required test signal pattern described above.
- Power on Sink DUT and verify that tested HDMI input is active.
- If Sink adequately support signal → PASS

Test ID 8-22: Audio Sample Packet Jitter

Reference	Requirement
[HDMI: 7.8.1] Packet Delivery Rules: Audio Sample Packets	"Relative to an ideal constant-frequency clock, the jitter present in the Audio Sample Packet transmission timing shall not exceed one horizontal line period plus a single audio sample period."

Test Objective

Verify that Sink supports Audio Sample Packets with maximum jitter.

Required Test Method

For each of the A/V formats described in 8.6.1 introduction above:

- [Verify reception of Audio Sample Packets with maximum jitter.]
- Transmit HDMI audio/video stream containing the following:
  - ACR packets contain the recommended N and CTS values per [HDMI: 7.2.3].
  - Audio Sample packet transmission timing has jitter of one horizontal video (total) line time plus the period of 1 audio sample (i.e. 1/Fs).
- Perform listening test
- If no sound, extraneous sound (e.g. clacking sound), or unnecessary mute (e.g. short term mute, etc) → FAIL

Recommended Test Method

For each of the A/V formats described in 8.6.1 above:

- Connect TPA-P-TDR to HDMI input connector of Sink DUT.
- Connect Tektronix DTG5274 to all TMDS differential pairs on the TPA-P-TDR.
- Configure the Tektronix DTG5274 to output required test signals described above.
- Power on Sink DUT and verify that tested HDMI input is active.
- If Sink adequately supports all tested signals → PASS

Test ID 8-23: Audio Formats

Reference	Requirement
[861B: 7.5] CEA EDID Timing Extension Version 3	"If audio is supported in the DTV Monitor, as indicated by the basic audio support bit in the Version 3 CEA EDID Timing Descriptor, then CEA short audio descriptors shall be used to declare which (if any) audio formats are supported in addition to basic audio." "If only basic audio is supported, no Short Audio Descriptors are necessary."
[HDMI: 8.3] E-EDID Data Structure	"…it is permitted for a Source to transmit Basic Audio (see Section 7.3) to a Sink that does not indicate support for Basic Audio."

Test Objective

Verify that Sink supports every audio format specified in EDID.

Required Test Method

The ATC is not required to test non-PCM formats.

- Determine EDID-advertised audio capabilities by examining Basic Audio bit (byte #3, bit#6 of CEA Timing Extension) and any Audio Data Blocks present.
- Transmit HDMI signal with 2-channel 32kHz PCM signal to Sink DUT
- If Sink DUT does not adequately support the audio format → FAIL
- Transmit HDMI signal with 2-channel 44.1kHz PCM signal to Sink DUT
- If Sink DUT does not adequately support the audio format → FAIL
- Transmit HDMI signal with 2-channel 48kHz PCM signal to Sink DUT
- If Sink DUT does not adequately support the audio format → FAIL
- For each audio format advertised in any Audio Data Block do the following:
  - Transmit that audio format at the maximum Sink-supported audio sampling frequency and with the maximum number of Sink-supported audio channels, to the Sink, in combination with 640x480p @ 59.94/60Hz.
  - If Sink does not adequately support the audio format → FAIL
- Repeat for remaining audio formats

Recommended Test Method

- Connect TPA-P-TDR to HDMI input connector of Sink DUT.
- Connect Tektronix DTG5274 to all TMDS differential pairs on the TPA-P-TDR.
- Configure the Tektronix DTG5274 to output required test signals described above.
- Power on Sink DUT and verify that tested HDMI input is active.
- If Sink adequately support signal for all tested signals → PASS

8.7 Sink – Interoperability With DVI

Test ID 8-24: Interoperability With DVI

Reference	Requirement
[HDMI: App. C.1] Requirement for DVI Compatibility	"…all HDMI Sinks shall be compatible with DVI 1.0 compliant sources (i.e. "systems" or "hosts") through the use of a similar cable converter."
[HDMI: App. C.3] HDMI Sink Requirements	"An HDMI Sink, upon power-up, reset or detection of a new source device, shall assume that the source device is limited to the above behavior. Upon the detection of an indication that the source is HDMI-capable, the HDMI Sink shall follow all of the HDMI Sink-related requirements specified in this document."

Test Objective

Verify that Sink DUT can handle required transition from DVI to HDMI mode.

Required Test Method

- Connect Sink DUT to Audio/Video Protocol Generator
- Transmit 720x480p or 720x576p, RGB pixel encoding, no Guard Bands, no Data Islands
- If Sink does not adequately support signal → FAIL

Recommended Test Method

- Connect Sink DUT to Audio/Video Protocol Generator
- Configure Audio/Video Protocol Generator to transmit stream with 720x480p or 720x576p, RGB pixel encoding, no Guard Bands, no Data Islands.
- Turn on Sink DUT and verify that HDMI port is active.
- Verify that Sink DUT supports signal with correct pixel encoding and no audio.
- If Sink does not adequately support signal → FAIL

9 Tests – Repeater

9.1 Repeater Products Overview

Repeaters consist of some number of HDMI input ports and some number of HDMI output ports. Typical HDMI Sink functionality is associated with the input ports and typical Source functionality is associated with the output ports.

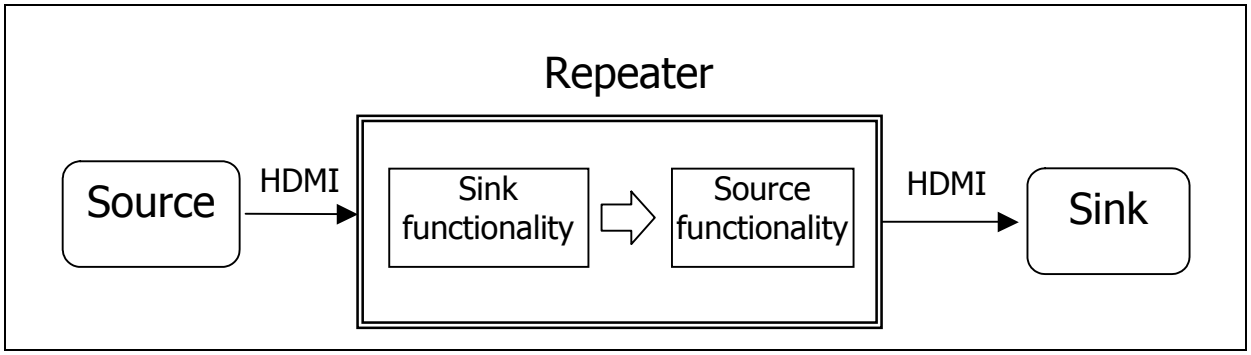


Figure 9-1 Repeater Products Overview

A compliant Repeater will consist of a product where each of the Source functional blocks is compliant with all of the HDMI Source requirements and each of the Sink functional blocks is compliant with all of the HDMI Sink requirements.

9.2 Internal Functional Block Categorization

Within the Repeater product, several functional blocks will be interacting during the transport of the A/V stream from the input port or ports to the output port or ports.

In order to more efficiently test Repeater products, it is useful to understand how these functional blocks interact within the tested product.

9.2.1 Input/Output Categories

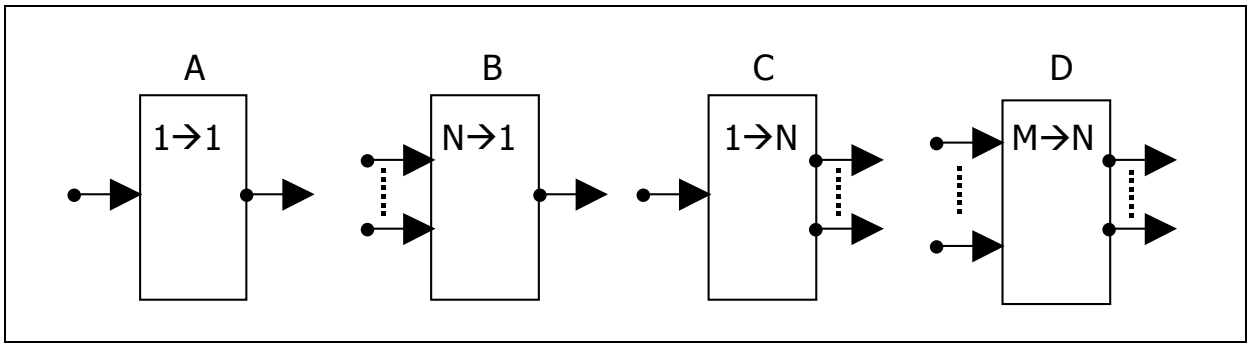


Figure 9-2 Input/Output Categories

Products will fall into several I/O categories:

a) 1→1 Content arriving on one input will be delivered to one output

b) N→1 Content arriving on more than one inputs will be combined in some manner and delivered to one output

c) 1→N Content arriving on one input will be delivered simultaneously to more than one output

d) M→N Content arriving on more than one input will be combined in some manner and delivered simultaneously to more than one output

9.2.2 Processing Categories

Internally the A/V stream may undergo one or more of the following types of processing:

a) Through A/V signal passes unmodified from Source to Sink.
EDID passes unmodified from Sink to Source.

b) Convert A/V signal is converted from format X to format Y. This could be, for instance, a video format conversion from HD to SD.
EDID corresponding to format Y would be present on the Sink and the EDID presented to the Source would include format X.

c) Switch A single A/V signal is selected from multiple Sources.
EDID from the Sink passes unmodified from Sink to Source.

d) Mix Multiple A/V signals are mixed. Example: a picture-in-picture function.
EDID from Sink is used for output processing and, depending upon capabilities of the main picture and the sub-picture processing, different EDIDs may be presented to different Sources.

e) Distribute Single A/V signal is sent, unmodified, to a single selected Sink.
EDID from single Sink passes unmodified to Source.

f) Duplicate Single A/V signal is passed unmodified to multiple Sinks.
EDID presented to Source may be the intersection of the sets of formats in each of the EDIDs in the multiple Sinks.

g) Exchange Multiple A/V signals pass from different Sources to different Sinks without any interaction between the streams.
EDIDs presented to Source correspond to Sink destination of that input's stream.

9.2.3 Combinations

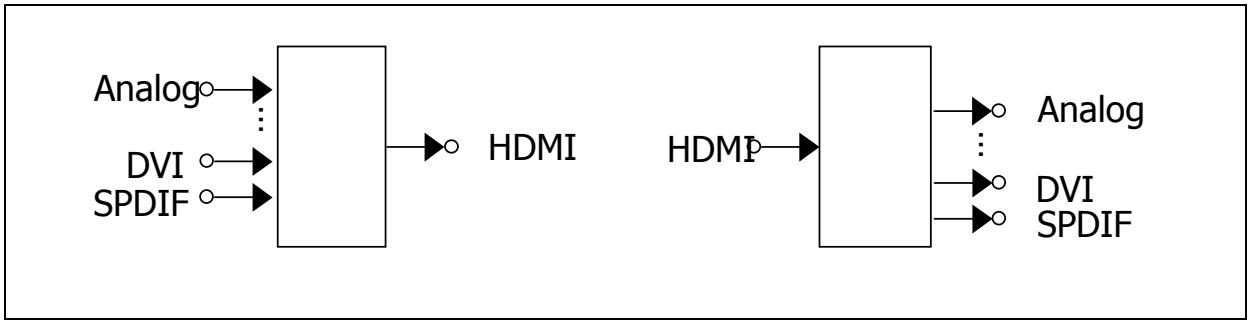
The following combinations of functional blocks are possible on each of the different I/O categories.

	Through	Convert	Switch	Mix	Distribute	Duplicate	Exchange
1→1	Y	Y					
N→1	Y	Y	Y	Y			
1→N	Y	Y			Y	Y	
M→N	Y	Y	Y	Y	Y	Y	Y

9.2.4 Non-HDMI I/O

In addition to HDMI input → HDMI output functionality, many Repeater products include the ability to source an A/V stream that was delivered to the Repeater on a non-HDMI (analog, DVI or other)

input. Likewise, many such products include the ability to forward an A/V stream from an HDMI input to a non-HDMI output.

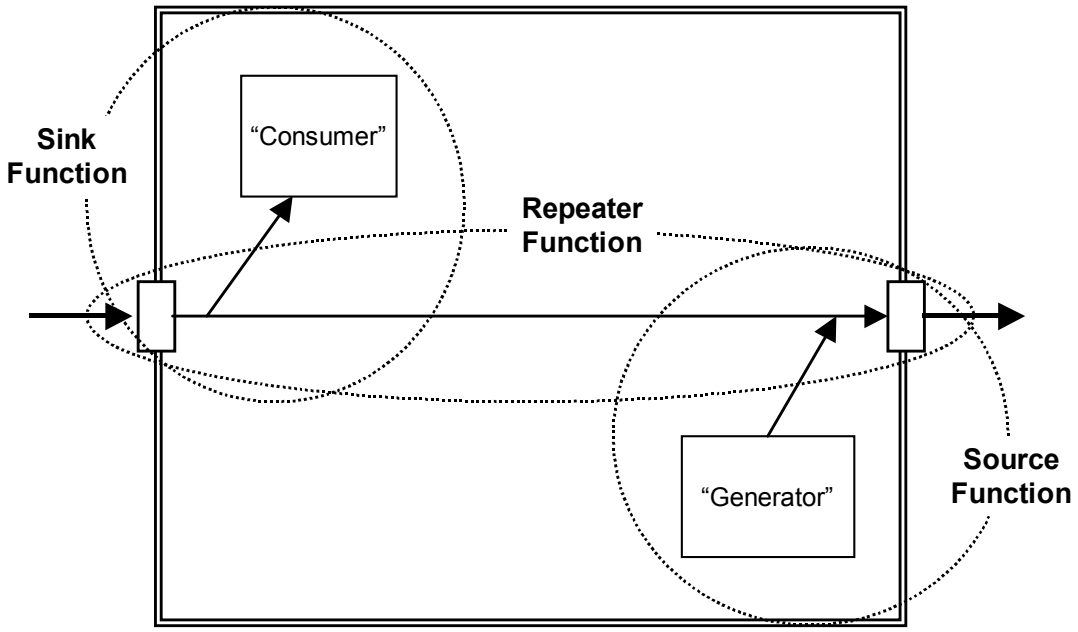


Such functionality is not addressed in this document.

9.2.5 Source / Sink / Repeater Functionality

Basic Repeater functionality associated with carrying an A/V stream from an HDMI input to an HDMI output is described above.

In addition, many such products also incorporate functions which require them to be tested more extensively.



An example are Repeater products that effectively act as Source products, where the HDMI stream has been "generated" through an internal function such as a DVD player or STB. Likewise, many products act as HDMI Sinks and "consume" the HDMI input stream by displaying it or routing to an audio amplifier for rendering.

HDMI Repeater functionality is tested below. For these tests, the Repeater CDF must be completed to describe the capabilities of the product. In addition, a mini (Source/Sink) CDF is required that describes a subset of the Source and Sink functionality of the product that is related to the Repeater function. This mini-CDF consists of the Source CDF and Sink CDF with many fields already filled-in.

The “generation” and “consuming” functions of a Repeater are tested as a Source and Sink device. For these tests, the normal Source or Sink CDF form must be completed indicating the characteristics of that Source or Sink function.

9.3 Tests of Output Ports

Test ID 9-1: Repeated Output Port

Test Objective

Verify that the HDMI output of an A/V stream from an HDMI input is compliant.

Required Test Method

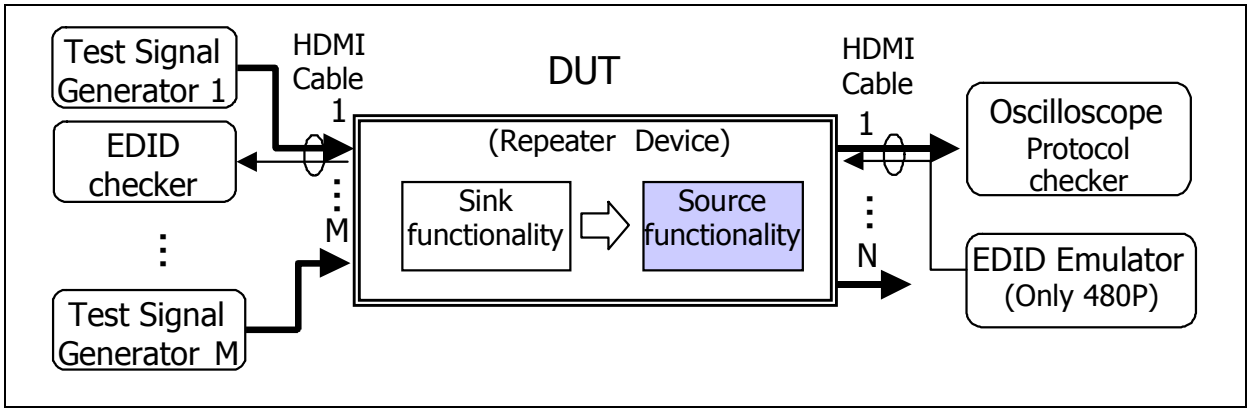


Figure 9-3 Testing of Source Functionality

- For each HDMI output port on DUT, do the following:
  - Determine which HDMI inputs may impact the behavior of the tested HDMI output based on the I/O categorization in CDF field Repeater_IO_Category. and the processing categorization indicated in CDF fields Repeater_Through through Repeater_Exchange.
  - Attach an Audio/Video Protocol Generator to each of the relevant HDMI input ports.
  - Configure and operate the Audio/Video Protocol Generator to generate a compliant video stream consisting of the following:
    - Either 720x480p @ 59.94Hz or 720x576p @ 50Hz (depending upon 50Hz/60Hz capability of product) and one of the HDTV formats supported by the product (if any – see CDF field Repeater_HDTV).
    - RGB pixel encoding
    - 48kHz, 2-channel PCM audio
  - Perform each test case in Section 7, Tests – Source, using the tested port as the HDMI Source DUT.
  - If any test item FAILs → FAIL
- Repeat for each of the HDMI output ports (total count equals CDF field CDF_HDMI_output_count)

Test ID 9-2: Sink Functionality

Test Objective

Verify that the Sink “consumer” functionality contained within a Repeater product is compliant.

Required Test Method

If the product contains a “consuming” function (described above), then Adopter must complete a full Sink CDF describing that function. In addition to the Repeated Port tests above, the following tests are required:

- If CDF field Repeater_Sink_Fn is ‘Y’ then do the following:
  - For each HDMI input port on DUT, do the following:
    - Perform each test case in Section 8, Tests – Sink, using the tested port as the HDMI Sink DUT and using the full Sink CDF.
    - If any test item FAILs → FAIL
  - Repeat for each of the HDMI input ports

9.4 Tests of Input Ports

Test ID 9-3: Repeated Input Port

Test Objective

Verify that the HDMI input of a stream that is transported to an HDMI output is compliant.

Required Test Method

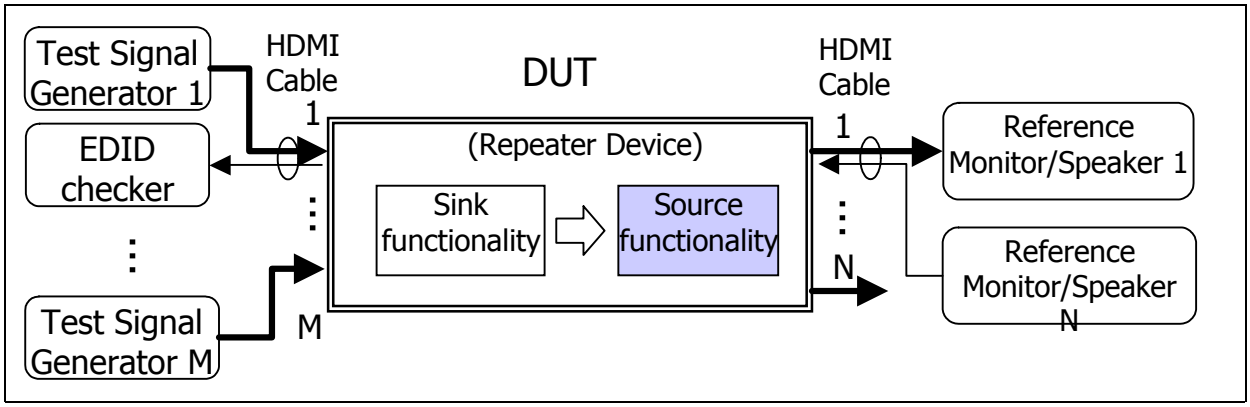


Figure 9-4 Testing of Sink Functionality

- For each HDMI input port on DUT, do the following:
  - Determine which HDMI outputs may be impacted by the tested HDMI input based on the I/O categorization in CDF field Repeater_IO_Category. and the processing categorization indicated in CDF fields Repeater_Through through Repeater_Exchange.
  - Attach a fully-compliant reference HDMI Monitor and Speaker to each relevant HDMI output.
  - Perform each test case in Section 8, Tests – Sink, using the tested port as the HDMI Sink DUT.
    - Connect and operate required test equipment (analyzers, etc.) to tested port, as specified in each test case.
  - If any test item FAILs → FAIL
- Repeat for each of the HDMI input ports (total count equals CDF field CDF_HDMI_input_count)

Test ID 9-4: Source Functionality

Test Objective

Verify that the Source "generator" functionality contained within a Repeater product is compliant.

Required Test Method

If the product contains a "generating" function (described above), then Adopter must complete a full Source CDF describing that function. In addition to the Repeated Port tests above, the following tests are required:

- If CDF field Repeater_Source_Fn is 'Y' then do the following:
  - For each HDMI input port on DUT, do the following:
    - Perform each test case in Section 7, Tests – Source, using the tested port as the HDMI Source DUT and using the full Source CDF.
    - If any test item FAILs → FAIL
  - Repeat for each of the HDMI output ports

9.5 Tests for Physical Address Handling

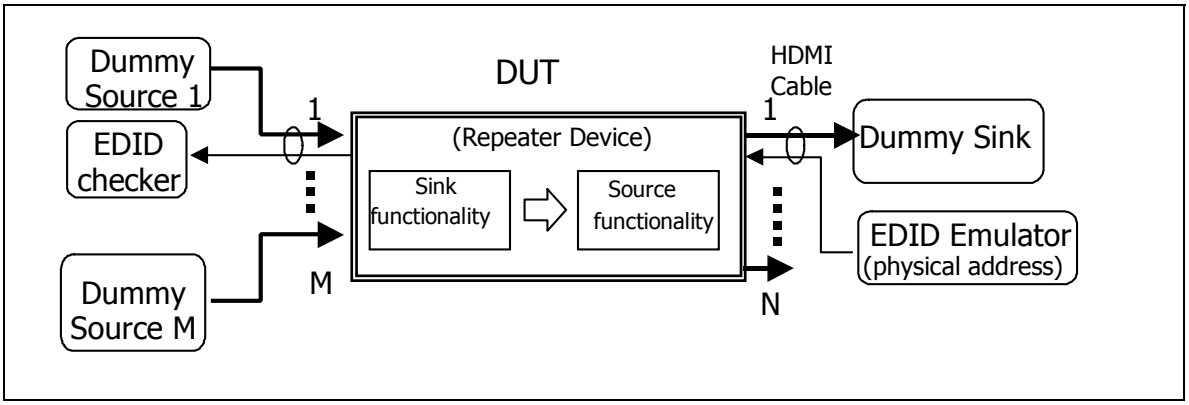
Test ID 9-5: Physical Address

Reference	Requirement
[HDMI: 8.7] Physical Address	<See reference for details.>

Test Objective

Verify that Repeater DUT supplies correct Physical Addresses to each of the attached Source devices.

Required Test Method



- Connect the EDID Emulator to the output port which is connected to the CEC signal, specified in CDF field Repeater_CEC_Output.
- For each of the HDMI input ports on the Repeater DUT:
  - Power on the DUT and verify that all relevant ports are active.
  - Connect the EDID Reader/Analyzer to the selected input port.
  - For each of the entries inTable 7-1, do the following:
    - Configure EDID Emulator to supply an EDID image indicating the “Sink Physical Address” shown in the table.
    - Using the EDID Reader/Analyzer, read and analyze the EDID image from the selected input port.
    - Compare the Physical Address read against the appropriate “Source Physical Address” value (based on the CDF fields Repeater_PA_Copy and Repeater_PA_Increment).
    - If the read Physical Address does not equal expected value → FAIL
  - Repeat for each of the remaining entries in the table.
- Repeat for each of the remaining input ports on the DUT.

Table 9-1 Physical Address Test

Sink Physical Address	Source Physical Address	
	Repeater_PA_Copy	Repeater_PA_Increment
1.0.0.0	1.0.0.0	1.M.0.0
2.0.0.0	2.0.0.0	2.M.0.0
2.3.0.0	2.3.0.0	2.3.M.0
3.4.5.0	3.4.5.0	3.4.5.M
1.1.1.1	1.1.1.1	F.F.F.F
F.F.F.F	F.F.F.F	F.F.F.F

Appendix 1 – Authorized Testing Center – Test Equipment List

The following is the equipment used in the Authorized Testing Centers in their initial operation.

TPA Fixtures

- Tektronix TPA-P-DI, available as one component in Tektronix 013-A013-50
- Tektronix TPA-P-SE, available as one component in Tektronix 013-A013-50
- Tektronix TPA-P-TDR, available as one component in Tektronix 013-A013-50
- Tektronix TPA-R-DI, available as one component in Tektronix 013-A012-50
- Tektronix TPA-R-SE, available as one component in Tektronix 013-A012-50
- Tektronix TPA-R-TDR, available as one component in Tektronix 013-A012-50
- ADVANTEST TPA-R-NA, part number CAX-ATI013

Jitter/Eye Analyzer

- Tektronix TDS7404 4GHz Digital Oscilloscope, with 32 mega-samples total (16 mega-samples on each of two active channels).
- (2) Tektronix P7330 Differential Probes
- PC running 32-bit Windows OS (may be integrated into oscilloscope)
- Tektronix SoftCRU software, running on the Windows PC, designed to be used with the data captured from the Tektronix TDS7404 digital oscilloscope. (See Appendix 2 for details.)

4GHz Digital Oscilloscope

- Tektronix TDS7404 4GHz Digital Oscilloscope with large memory option (#4M)

Differential Probe

- Tektronix P7330 Differential Probe
- Tektronix 016-1884-00 Square Pin Adapter
- Tektronix 196-3469-00 Ground Lead

Single-Ended Probe

- Tektronix P7240
- Tektronix 016-1773-00 Square pin socket

SMA Cables

- Tektronix 174-1428-00 (1.5 meter)
- Tektronix 174-1341-00 (1 meter)

TMDS Signal Generator

- (1) Tektronix DTG5274 2.7GHz Digital Timing Generator (DTG)
- (3) Tektronix DTGM30 output modules for DTG5274
- (2) Tektronix 012-1503-00 Pin Header SMB 51cm (20in.)
- (2) Tektronix 015-0671-00 SMB-BNC adapter
- (1) Tektronix AWG710 Arbitrary Waveform Generator
- (2) Mini-circuits ZFBT-4R2GW Bias-Tee
- (2) BNC-SMA adapters (1 for each Bias-Tee)
- (1) TPA-P-TDR (in some test configurations, where driving a Sink directly)
- (1) TPA-R-TDR (in some test configurations, where driving a cable)
- (12) SMA Cables: Tektronix 174-1428-00 (1.5 meter) and Tektronix 174-1341-00 (1 meter), as needed to connect output of equipment to TPA boards and to deliver synchronization signal(s) from AWG to DTG

Network Analyzer

- ADVANTEST R3860
- ADVANTEST R17051 (Auto Cal KIT)

TDR/TDT Oscilloscope

- Tektronix TDS8000B
- Tektronix 80E04 TDR-module
- Tektronix 80E03 Sampling module

Digital Multi-Meter and Probe

- ADVANTEST R6240A

Voltage Meter

- ADVANTEST R6552

DC power supply

- KENWOOD PW18-1.8AQ

LCR Meter

- HIOKI 3522-50 Digital LCR Meter
- HIOKI 9143 Probe
- HIOKI 9268 DC Bias unit

HDMI Cable Emulator

- For 74.25MHz tests: JAE DC1P19ST07425AA
- For 27MHz tests: JAE DC1P19ST02700AA

EDID Reader/Analyzer + EDID Emulator

- Silicon Image EDID Tester PCB.
- PC running Windows 32-bit OS.
- Serial cable.
- Silicon Image EDID Analyzer / Editor Software

I^2C Analyzer

- Yokogawa DL1640/F5 Oscilloscope (includes I2C Analyzer option)

Protocol/Audio/Video Analyzer

- TMDS Capture Board
- Personal Computer running a Windows 32-bit OS with an IEEE1394 port available and connected to the TMDS Capture Board.
- HDMI Analysis Software running on the PC
- IEEE1394 cable connected between TMDS Capture Board and PC

Encoding Analyzer

- Protocol/Audio/Video Analyzer described above

Protocol Analyzer

- Protocol/Audio/Video Analyzer described above

Video Timing Analyzer

- Protocol/Audio/Video Analyzer described above

Video Picture Analyzers

- Protocol/Audio/Video Analyzer described above

Audio Timing Analyzer

- Protocol/Audio/Video Analyzer described above

TMDS Protocol Generator

- Tektronix DTG5274 Digital Pattern/Timing Generator
- Tektronix DTM30 (3pcs) output module for DTG5274
- Tektronix 174-1428-00 SMA cable
- TPA-P-TDR (in some test configurations, where driving a Sink directly)
- SMA Cables as needed to connect output of equipment to TPA boards

Audio/Video Protocol Generator

- Tektronix DTG5274 Digital Pattern/Timing Generator
- Tektronix DTGM30 (3pcs) output module for DTG5274
- Tektronix 174-1428-00 SMA cable

Appendix 2 – Software CRU Technology

(Informative)

The HDMI specification mandates the Clock Recovery Unit (CRU) utilizing a Phase Locked Loop (PLL) with first order transfer function characteristics, in the measurement of the jitter and the eye diagram[1]. The use of a PLL based CRU implemented in hardware has the drawback that correlation of measurement results is difficult due to differences in vendor specific implementations. There are software PLL techniques that exist to extract clock and timing data from a serial data stream. One such technique uses a time domain convolution integral technique that can address the requirement, however this technique demands very high performance digital processing. The method proposed in this paper shows a more practical and affordable way to satisfy the requirement. [2]

PLL Characteristics

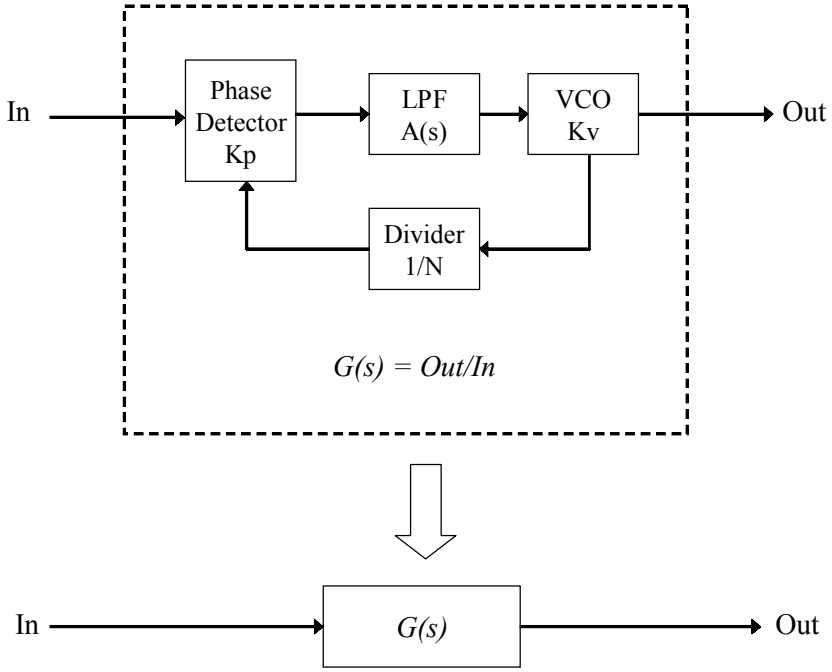


Fig.1 PLL Functional Block

Fig. 1 shows a simplified block diagram of generic phase locked loop (PLL). A PLL consists of the Phase Detector (PD), Low Pass Filter (LPF), Voltage Controlled Oscillator (VCO) and Frequency Divider (FD).

[1] Refer to section 4.2.3 of HDMI Specification Version 1.0

[2] This Technology is provided by Tektronix Inc..

The phase of the input signal is compared to the phase of FD output. The input of the FD is the output of VCO, whose frequency is controlled by the LPF output, which is a filtered form of the PD output. When the phase of FD output is leading compared to the input phase, the PD output changes to decrease the VCO frequency, thus the FD output will lag. Due to the effect of this feedback mechanism, the frequency of VCO is locked to N-times of the input frequency.

As the LPF restricts the quick variation of the incoming signal, high frequency changes in the input phase will be attenuated before being transferred to consecutive functional blocks. Therefore the VCO output represents the average phase of input signal even if the input signal does not have the constant phase rotation i.e. frequency. Using this approach, the PLL circuitry is able to recover the clock information from the modulated input signal.

The transfer function from the input phase to the output phase is represented by following equation:

$$G(s) = \frac{\frac{Kp \cdot Kv \cdot H(s)}{s}}{1 + \frac{Kp \cdot Kv \cdot H(s)}{s \cdot N}} = \frac{N \cdot Kp \cdot Kv \cdot H(s)}{s \cdot N + Kp \cdot Kv \cdot H(s)}$$

Where Kp and Kv are the sensitivity coefficients of PD and VCO respectively, and N is the division factor of FD. H(s) is the transfer function of LPF in the frequency domain.

Assuming N, Kp and Kv are constant, the function G(s) can be simplified as follows:

$$G(s) = \frac{K_2 \cdot H(s)}{s + K_1 \cdot H(s)}$$

It should be noted that G(s) becomes the first order low-pass filter only when H(s) is constant, namely when H(s) is non-dependent on the frequency. This means that H(s) is no longer a low-pass filter in this case. On the contrary, it is well known that the PLL will not be stable without low-pass filter in place of H(s). Therefore the first order transfer function which is required by CRU for HDMI may not be realized by the PLL circuitry shown in Fig.1.

Conventional Method

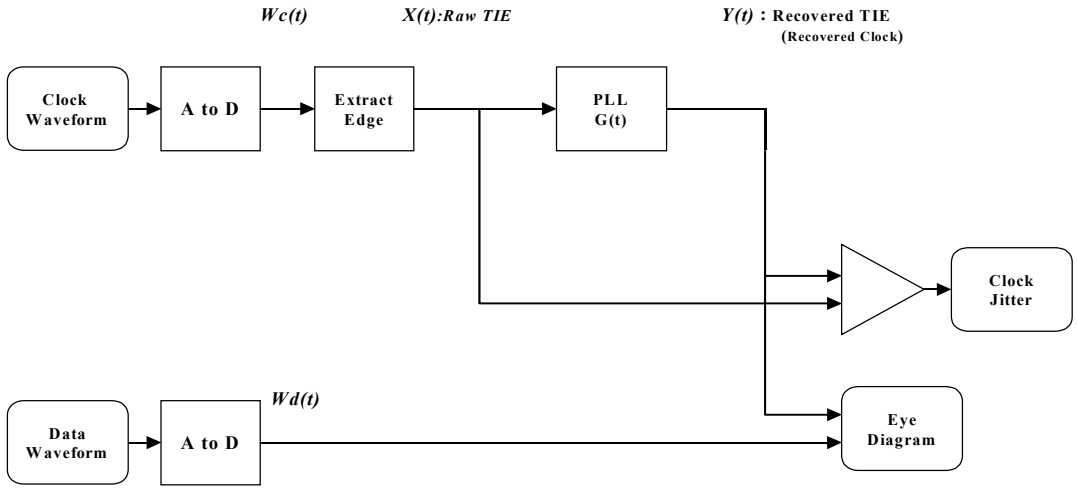


Fig.2 Conventional Clock Recovery Method

Fig. 2 shows a simple PLL design for CRU, measuring clock jitter and eye diagram within a digital oscilloscope. The input signal is first converted to digital information with an A/D converter. The phase of the input signal is extracted by finding the rising (or falling) edges of the digitized signal. A digital simulation of an actual hardware PLL circuit may be realized because the input and output signals exist as just digital information. In this case, the voltage values at several points in the PLL circuit are expressed in the time domain, and are repetitively calculated to derive their time variation. The time interval of the calculation must be sufficiently small in order to retain the high precision of the simulation. Hence it requires significant amount of digital processing capability to simulate actual PLL within a reasonable amount of time.

In this method, the phase transfer function of the PLL is determined by the characteristics of the simulated components. As long as the simulation observes the law of physics, the resultant transfer function does not differ from that of the actual hardware PLL circuit. Given the time to process the data in the simulation, using this method is not advisable. Hence the first order transfer function to be realized by this method may not be useful too.

Another method to simulate a PLL in software is to use its time domain transfer function from the input phase error to output timing information. The impulse response is used as the time domain transfer function. In this case, given the input signal X(t), the integral operation shown below gives the output signal Y(t).

$$Y(t) = \int_{\tau=-\infty}^{\infty} X(t) \cdot G(\tau - t) d\tau$$

Where G(t) is the time domain representation of G(s) mentioned in the previous section. This is so-called convolution integral. In this case the input signal is represented as discrete-time samples. The integration above should also be performed in discrete fashion as follows.

$$y(n) = \sum_{m=-\infty}^{\infty} g(m) \cdot x(n-m) = \sum_{m=-\infty}^{\infty} g(n-m) \cdot x(m)$$

There are two disadvantages in time domain convolution method. One is that it still requires a huge number of multiplications and additions to calculate the values of all time points, as easily seen from the form of the equation above. Another is that it is not always practical to express the time domain transfer function as an explicit mathematical representation. In many cases, the human interpretation of the transfer function is made in frequency domain. Some means of conversion is required to derive the time domain response from the frequency domain characteristics. This requirement will complicate the design of the user interface.

It is important to mention that the first order transfer function characteristics can be realized by this convolution method, while it has the difficulties described above. Also important is that this method is inherently stable as far as an appropriate impulse response is adopted, because it does not include any feedback loop.

Proposed Method

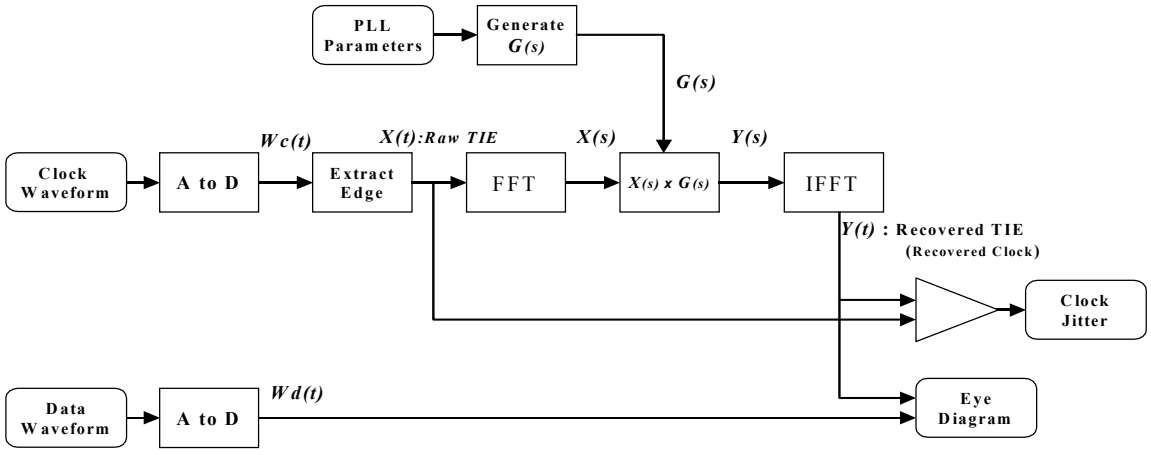


Fig.3 Proposed Clock Recovery Method

The PLL circuitry acts in whole as a low pass filter for incoming time information. In the frequency domain the filter function is simply realized by multiplication of the frequency response coefficients to the input spectrum. The convolution integral in the time domain is equivalent to simple multiplication between frequency-domain functions derived by the well-known Fourier Transform. If the time information and the PLL characteristics are transformed to frequency domain, the PLL processing becomes much easier than in the time domain.

$$Y(s) = G(s) \cdot X(s)$$

As seen in the above equation, the calculation becomes one multiplication (though between complex numbers) per sample point. Hence it keeps the demand for digital processing performance very low.

After filter function is performed, the time information of the output signal may be derived with inverse transformation. Using FFT algorithm the forward and inverse transformation can be executed in relatively short time compared to simulation in time domain. Thus the total time to calculate the recovered clock can be significantly reduced.

Jitter Measurement

The jitter of the incoming clock signal is measured by statistically analyzing the time difference between the incoming and recovered clocks. As the timing information of both signals is already retained in digital form, the jitter calculation is simple and straightforward. Usually the peak-to-peak jitter value and the standard deviation (i.e. RMS) jitter value are used for evaluating the signal quality.

$$Jpp = \Delta T \max - \Delta T \min$$

$$J\sigma = \sqrt{\frac{\sum \left(\Delta T_n - \overline{\Delta T}\right)^2}{N}}$$

Appropriate sample points should be chosen to measure the jitter for specific case such as the clock-to-data jitter at the first bit. Such a requirement is addressed by specifying a rectangular area with time range of [–T..+T] and voltage range of [-V..+V].
To obtain an accurate measurement, a large number of samples are required. As the area restriction above reduces the number of measured samples, the capability to process more and more samples is desired. Using the proposed method, it becomes realistic to gather huge amount of statistical information for more precise measurement.

Eye Diagram

An eye diagram is the incoming data waveform repeatedly drawn with the recovered clock used as the time reference. The recovered clock is represented as time information hence it may be used to derive the position where the input data waveform should be drawn. The resulting diagram will precisely indicate the true marginal area with which the reliability of data transmission is determined.

The vertical coordinate to draw the incoming waveform is determined by using the data value itself. To draw the horizontal coordinate (x) is determined by the following equation.

$$Xcoord = Tn - Tref$$

Where, Tn is the time of incoming waveform, and Tref is the time of the reference signal, i.e. the recovered clock signal.

Appendix 3 – Capabilities Declaration Form (CDF)

The following declaration must be completed prior to testing. The options that are supported will be used to determine which groups of tests are performed.

Product Category

Field Name	***Field Definition***	***Choices***
CDF_HDMI_output_count	How many HDMI output ports are on product?	0…X
CDF_HDMI_input_count	How many HDMI input ports are on product?	0…X
CDF_CEC	CEC supported?	Y/N

Source Capabilities

A copy of the following table must be completed for each of the HDMI output ports on the product (field CDF_HDMI_output_count, above). If a group of ports have identical capabilities, only one form needs to be completed for that group. Please indicate which ports are covered by which form.

Which HDMI output ports are covered by this form?	
Is this form a min-CDF meant for Repeater functionality testing?	

Field Name	***Field Definition***	***Choices***	***Repeater Mini-CDF***
Video			
Source_HDMI_YC_BC_R	Will the product transmit an HDMI video signal using YC_BC_R (4:4:4 or 4:2:2) pixel encoding under some conditions (user selection, EDID indication etc.)?	Y/N	<Adopter fills in field>
Source_AVI_Required	Per EIA/CEA-861B-rules, is the product ever required to transmit an AVI InfoFrame?	Y/N	<Adopter fills in field>
Source_AVI_Supported	Does the product support the transmission of the AVI InfoFrame under some conditions?	Y/N	<Adopter fills in field>
Source_AVI_Info_Available	Is any of the following information available and valid at the Source?: 'Active Format Aspect Ratio,' bar widths, overscan vs. underscan, non-uniform picture scaling, or the colorimetry of the video.	Y/N	N
Source_Alt_Colorimetry	Will the product ever transmit video using a non-default (i.e. alternate) colorimetry under some condition? (e.g. using BT.709 for 480p or BT.601 for 1080i).	Y/N	N
Source_60Hz	Does the product output standard, enhanced or high-definition 60Hz video formats on any video output in addition to 640x480p @ 60Hz?	Y/N	N
Source_50Hz	Does the product output standard, enhanced or high-definition 50Hz video formats on any video output?	Y/N	N

Field Name	***Field Definition***	***Choices***	***Repeater Mini-CDF***
Source_861B_Formats	Which EIA/CEA-861B video formats are supported by product?	861B format numbers (1…34)	2 (if 60Hz product) 17 (if 50Hz product)
Source_Non-861B_Formats	Can the product support formats that are not described by EIA/CEA-861B?	Y/N	N
Source_DTD_1	Can this product support any format not described in EIA/CEA-861B that is in the first Detailed Timing Descriptor?	Y/N	N
Source_DTD_2_end	Can this product support any format not described in EIA/CEA-861B that is listed only in a Detailed Timing Descriptor other than the 1st DTD?	Y/N	N
Source_Standard-Timings	Can this product support any format not described in EIA/CEA-861B that is listed only in the EDID Standard Timings field?	Y/N	N
Source_Established-Timings	Can this product support any format not described in EIA/CEA-861B that is listed only in the EDID Established Timings field?	Y/N	N
Source_720p60	Tested Format : 1280x720p @ 59.94/60Hz Is DUT capable of transmitting Tested Format using any other component analog or uncompressed digital video output?	Y/N	N
Source_1080i60	Tested Format : 1920x1080i @ 59.94/60Hz Is DUT capable of transmitting Tested Format using any other component analog or uncompressed digital video output?	Y/N	N

Field Name	***Field Definition***	***Choices***	***Repeater Mini-CDF***
Source_480p60	Tested Format : 720x480p @ 59.94/60Hz Is DUT capable of transmitting Tested Format using any other component analog or uncompressed digital video output?	Y/N	N
Source_720p50	Tested Format : 1280x720p @ 50Hz Is DUT is capable of transmitting Tested Format using any other component analog or uncompressed digital video output?	Y/N	N
Source_1080i50	Tested Format : 1920x1080i @ 50Hz Is DUT capable of transmitting Tested Format using any other component analog or uncompressed digital video output?	Y/N	N
Source_576p50	Tested Format : 720x576p @ 50Hz Is DUT capable of transmitting Tested Format using any other component analog or uncompressed digital video output?	Y/N	N

Field Name	***Field Definition***	***Choices***	***Repeater Mini-CDF***
Audio			
Source_Basic_Audio	"Basic Audio" supported?	Y/N	Y
Source_PCM_Channels	Max supported L-PCM Channel Count	0, 2…8 channels	2 channels
Source_PCM_Primary_Fs	L-PCM Primary Freq	32kHz, 44.1kHz, and/or 48kHz	48kHz
	Under what conditions can above occur	<Media required, signal input required, UI actions, etc.>	Always
Source_PCM_Max_Fs	L-PCM Maximum Freq	32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz, and/or 192kHz	48kHz
	Under what conditions can above occur	<Media required, signal input required, UI actions, etc.>	Always
Source_NonPCM_Types	Additional audio Coding Types supported	'None' or 861B Table 19 CT values: 0…8	None
Source_NonPCM_MaxFs	Maximum Fs for non-PCM formats	N/A, 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz, or 192kHz	N/A

Sink Capabilities

A copy of the following must be completed for each of the HDMI input ports on the product (field CDF_HDMI_input_count, above). If a group of ports have identical capabilities, only one form needs to be completed for that group. Please indicate which ports are covered by which form.

Which HDMI input ports are covered by this form?	
Is this form a min-CDF meant for Repeater functionality testing?	

Field Name	***Field Definition***	***Choices***	***Repeater Mini-CDF***
Electrical			
Sink_Diff_PowerOn	Does the product require that power is applied when termination impedance is measured?	Y/N	<Adopter fills in field>
Sink_Term_Distance	If Sink_Diff_PowerOn is 'Y' then: For an impedance measurement, what is the length that can be correctly measured with power off? The length is defined as the number of nsecs it takes for a pulse to travel from the input connector, begin to reflect from the termination impedance, and travel back to the input connector.	<any number>	<Adopter fills in field>
Video < For video format support, refer to EDID >			
Sink_Display	Does the device display video?	Y/N	<Adopter fills in field>
Sink_PrimaryAR	Is the device displays video, what is the primary aspect ratio of display?	4:3, 16:9	Ignore test case item.
Sink_HDTV	Does the device support HDTV capability?	Y/N	<Adopter fills in field>
Sink_YUV_On_Other	Is the product capable of receiving a color-difference color space across any other component analog or digital video interface?	Y/N	<Adopter fills in field>
Sink_60Hz	Does the product support standard, enhanced or high-definition 60Hz video formats on any video input in addition to 640x480p @ 60Hz?	Y/N	<Adopter fills in field>
Sink_50Hz	Does the product support standard, enhanced or high-definition 50Hz video formats on any video input?	Y/N	<Adopter fills in field>

Field Name	***Field Definition***	***Choices***	***Repeater Mini-CDF***
Sink_720p60	Tested Format : 1280x720p @ 59.94/60Hz Is DUT capable of supporting Tested Format using any other component analog or uncompressed digital video output?	Y/N	N
Sink_1080i60	Tested Format : 1920x1080i @ 59.94/60Hz Is DUT capable of supporting Tested Format using any other component analog or uncompressed digital video output?	Y/N	N
Sink_480p60	Tested Format : 720x480p @ 59.94/60Hz Is DUT capable of supporting Tested Format using any other component analog or uncompressed digital video output?	Y/N	N
Sink_720p50	Tested Format : 1280x720p @ 50Hz Is DUT is capable of supporting Tested Format using any other component analog or uncompressed digital video output?	Y/N	N
Sink_1080i50	Tested Format : 1920x1080i @ 50Hz Is DUT capable of supporting Tested Format using any other component analog or uncompressed digital video output?	Y/N	N
Sink_576p50	Tested Format : 720x576p @ 50Hz Is DUT capable of supporting Tested Format using any other component analog or uncompressed digital video output?	Y/N	N
Audio < For audio format support, refer to EDID >			
Sink_Audio_Input	Any analog or (non-HDMI) digital audio inputs on device or audio embedded on other combination (audio+video) input?	Y/N	Y

Repeater Capabilities

If the Repeater product is capable of acting as an is required to submit a Source CDF and a Sink CDF for the product as well as the Repeater CDF below.

Field Name	***Field Definition***	***Choices***
Categories		
Repeater_Source_Fn	Does the product contain an A/V generating function (such as STB or DVD player)?	Y/N
Repeater_Sink_Fn	Does the product contain an audio or video consuming function, such as a display or an audio amplifier?	Y/N
Repeater_IO_Category	Which I/O category applies to the product?	a, b, c, d
Repeater_Through	Does product include a 'Through' processing block?	Y/N
Repeater_Convert	Does product include a 'Convert' processing block?	Y/N
Repeater_Switch	Does product include a 'Switch' processing block?	Y/N
Repeater_Mix	Does product include a 'Mix' processing block?	Y/N
Repeater_Distribute	Does product include a 'Distribute' processing block?	Y/N
Repeater_Duplicate	Does product include a 'Duplicate' processing block?	Y/N
Repeater_Exchange	Does product include a 'Exchange' processing block?	Y/N
Video		
Repeater_HDTV	Which HDTV formats does Repeater function support?	<861B video code>
Audio		
Repeater_AudioPass	Audio passed-through Repeater?	Y/N
Repeater_AudioRender	Audio rendered on Repeater? (If Yes, fill out Sink audio handling section above for rendered audio formats)	Y/N
CEC		
Repeater_CEC	CEC supported?	
Repeater_CEC_Output	Which output port is connected to CEC?	<port name or number>
Repeater_PA_Copy	Does Physical Address simply get copied from the Sink to the internal EDID (simple repeater case)?	Y/N
Repeater_PA_Increment	Does Physical Address get incremented for each input port?	Y/N

Cable Assembly Capabilities

Field Name	***Field Definition***	***Choices***
Cable_Wire	Is cable constructed only of passive wire components (e.g. is it a typical copper cable)?	Y/N
Cable_Unidirectional	For proper operation does cable require specific end to be connected to Source device?	Y/N

Appendix 4 – Test Results Form

All Source DUT tests are performed for each output connector on a device therefore, a product with multiple output connectors will require the completion and submission of multiple Source DUT Test Results Forms. This holds true for input connectors on Sink products as well.

The testing of the ”Repeater” functionality of Repeater products requires the completion of a Source results form for each output connector and a Sink results form for each input as well as one Sink form for each port tested for “Consumer” and one Source form for “Generator” functionality (See Section 9, Tests – Repeater for details). In addition a Repeater results form is required.

Test Results Form – Source DUT

[Output Port: _____]

ID	Pass/Fail	Comment
7-1: EDID-Related Behavior		
7-2: TMDS $-V_L$		V_{L_MAX} = V D0+ = V, D0- = V D1+ = V, D1- = V D2+ = V, D2- = V CK+ = V, CK- = V
7-3: TMDS – I_{OFF}		I_{OFF} (microamps) D0+ = D0- = D1+ = D1- = D2+ = D2- = CK+ = CK- =
7-4: TMDS – T_{RISE}, T_{FALL}		T_{RISE} T_{FALL} D0: psec (T_{BIT}), psec (T_{BIT}) D1: psec (T_{BIT}), psec (T_{BIT}) D2: psec (T_{BIT}), psec (T_{BIT}) CK: psec (T_{BIT}), psec (T_{BIT})
7-5: TMDS – Ov/Undershoot		Overshoot = % Undershoot = %
7-6: TMDS – Inter-Pair Skew		T_{IPSKEW_MAX} = T_{PIXEL} D0-D1: D1-D2: D0-D2: D1-CK: D0-CK: D2-CK:

ID	Pass/Fail	Comment
7-7: TMDS – Intra-Pair Skew		T_{XPSKEW_MAX} = T_{BIT} D0: D1: D2: CK:
7-8: TMDS – Clock Duty Cycle		Clock Duty: Min = % Max = %
7-9: TMDS – Clock Jitter		Clock Jitter = T_{BIT}
7-10: TMDS – Eye Diagram		D Jitter = T_{BIT}
7-11: +5V Power		55mA: V_{5V} = V 0mA: V_{5V} = V
7-12: Hot Plug Detect		V_{HPD}(LOW) = V V_{HPD}(HIGH) = V
7-13: DDC/CEC Capacitance		SDA: C1= pF, C2= pF C_{SOURCE} = pF SCL: C1= pF, C2= pF C_{SOURCE} = pF CEC: C1= pF, C2= pF C_{SOURCE} = pF
7-14: CEC Line Connectivity		
7-15: CEC Line Degradation		
7-16: Legal Codes		
7-17: Basic Protocol		
7-18: Extended Control Period		

ID	Pass/Fail	Comment
7-19: Packet Types		
7-20: Type A Connector Usage		
7-21: Min Format Support		
7-22: Add'l Format Support		
7-23: RGB to RGB-only Sink		
7-24: YC_BC_R to YC_BC_R Sink		
7-25: Video Format Timing		
7-26: Pixel Repetition		
7-27: AVI InfoFrame		
<Audio Tests>		Tested A/V Format Combinations: 1) Video = Audio = 2) Video = Audio = 3) Video = Audio =
7-28: IEC 60958/IEC 61937		
7-29: ACR		
7-30: Audio Packet Jitter		
7-31: Audio InfoFrame		
7-32: Audio Packet Layout		
7-33: Interoperability With DVI		

Test Results Form – Sink DUT

[Input Port:_____]

The Test Results Form for each Sink DUT port tester also includes an EDID image in both of the following formats:

- Text file or human-readable format in hexadecimal with 16 bytes per line. Preferably this file will be interpreted, in-line, with a software tool such as the Silicon Image EDID Analyzer.
- Binary file in Intel Hex format

ID	Pass/Fail	Comment or Value
8-1: EDID Readable		
8-2: EDID VESA Structure		
8-3 CEA Timing Extension Structure		
8-4 TMDS – Termination Voltage		V_{TERM_MAX} = V D0+ = V, D0- = V D1+ = V, D1- = V D2+ = V, D2- = V CK+ = V, CK- = V
8-5: TMDS – Minimum Differential Sensitivity		V_{ICM}=3.00V : V_{DIFF} (minimum) = mV V_{ICM}=3.13V : V_{DIFF} (minimum) = mV
8-6: TMDS – Intra-Pair Skew		Format: x @ Hz (MHz) T_{IPSKEW_MAX}: D0: nS = T_{BIT} D1: nS = T_{BIT} D2: nS = T_{BIT} CK: nS = T_{BIT}

ID	Pass/Fail	Comment
8-7: TMDS – Jitter Tolerance		Format: x @ Hz (MHz) Max D_JITTER: nS = T_{BIT} Max C_JITTER: nS = T_{BIT}
8-8: TMDS – Differential Impedance		D0: Z_{DIFF_HI} = V, Z_{DIFF_LO} = V D1: Z_{DIFF_HI} = V, Z_{DIFF_LO} = V D2: Z_{DIFF_HI} = V, Z_{DIFF_LO} = V CK: Z_{DIFF_HI} = V, Z_{DIFF_LO} = V
8-9: DDC/CEC Line Capacitance		SDA: C1= pF, C2= pF C_{SINK} = pF SCL: C1= pF, C2= pF C_{SINK} = pF CEC: C1= pF, C2= pF C_{SINK} = pF
8-10: HPD Output Voltage		+5VP=0.0V : V_{HPD} = V +5VP=5.1V : V_{HPD} = V
8-11: HPD Output Resistance		V_A = , V_B = , Z_{HPD} = ohms
8-12: +5V Power Max Current		Powered On : V Powered Off : V Unplugged from AC: V
8-13: CEC Line Connectivity		
8-14: CEC Line Degradation		
8-15: Character Synchronization		

ID	Pass/Fail	Comment
8-16: Acceptance of All Valid Packet Types		
8-17: 861B Format Support Requirements		
8-18: HDMI Format Support Requirements		
8-19: Pixel Encoding Requirements		
8-20: Video Format Timing		Failed format: x @ Hz, Failed Min or Max frequency (circle) Failed format: x @ Hz, Failed Min or Max frequency (circle) Failed format: x @ Hz, Failed Min or Max frequency (circle)
8-21: Audio Clock Regen.		
8-22: Sample Packet Jitter		
8-23: Audio Formats		
8-24: Interoperability With DVI		

Test Results Form – Repeater DUT

ID	Pass/Fail	Comment
9-1: Repeated Output Port		
9-2: Sink Functionality		
9-3: Repeated Input Port		
9-4: Source Functionality		
9-5: Physical Address		

Test Results Form – Cable Assembly DUT

ID	Pass/Fail	Comment
5-1: Connector Minimum Envelope		
5-2: Wire Assignment		
5-3: TMDS Data Eye Diagram		
5-4: Intra-Pair Skew		T_{XPSKEW_MAX} = nS = T_{BIT}
5-5: Inter-Pair Skew		T_{IPSKEW_MAX} = nS = T_{BIT}
5-6: Far End Crosstalk		XFE D0-D1: dB, D1-D2: dB D0-D2: dB, D1-CK: dB D0-CK: dB, D2-CK: dB
5-7: Attenuation		A_{LOW} A_{MID} A_{HIGH} D0: dB, dB, dB D1: dB, dB, dB D2: dB, dB, dB CK: dB, dB, dB
5-8: Differential Impedance		

Test Results Form – Plug & Receptacle

ID	Pass/Fail	Comment
6-1: Connector Mechanical		
6-2: GROUP1 Environmental		
6-3: GROUP2 Mated Mechanical		
6-4: GROUP 3 Insulator Integrity		
6-5: GROUP4 Cable Flexing		
6-6: GROUP 5 Electrostatic		