Video Electronics Standards Association

E-EDID™

39899 Balentine Drive, Suite 125
Newark, CA 94560

Phone: 510 651 5122
Fax: 510 651 5127

VESA ENHANCED EXTENDED DISPLAY IDENTIFICATION DATA STANDARD

(Defines EDID Structure Version 1, Revision 4)

Release A, Revision 2
September 25, 2006

Purpose

The E-EDID Standard defines a remotely readable (read by a source) data file stored in an electronic display. The data in this file identifies the characteristics, features and video timing modes supported by the display product. The purpose of this standard is to describe the BASE (block 0) 128-byte data structure "EDID 1.4" (shorthand for EDID Version 1, Revision 4), as well as the overall layout of the data blocks that make up Enhanced EDID. This document specifies the ELEMENTS, data structures and file formats used to organize and store this data. The contents of this data file are used by a video source to configure its graphics processing unit to generate correctly formatted video for the display and to provide additional information for certain application programs.

Summary

This revision to the E-EDID Standard adds support for Consumer Electronic Products (Model Year and Aspect Ratio) and PC Products (CVT {Coordinated Video Timing}, Established Timings III, Additional Video Interfaces, Expanded Display Range Limits, optional Product Features and Timing Mode Priorities). This document contains specifications for the mandatory and optional elements of BASE EDID. These data formats are designed to support both computer based products and digital television products. Optional EDID EXTENSIONs are defined in separate VESA & CEA Standards.

Note: This document supersedes all previous versions of the EDID and E-EDID Standards.

The EDID 1.4 structure is intended to be backward compatible (key ELEMENTS only) with EDID structures 1.0, 1.1, 1.2 and 1.3 as implemented in most commercially available displays.

This document contains specifications for the mandatory core ELEMENTS of Enhanced EDID. Optional EDID extensions are defined in separate documents. Use of EDID extensions described in this document requires that the addressing methods described in the E-DDC (Enhanced Display Data Channel) Standard are used.

Preface

Intellectual Property

While every precaution has been taken in the preparation of this standard, the Video Electronics Standards Association and its contributors assume no responsibility for errors or omissions, and make no warranties, expressed or implied, of functionality or suitability for any purpose.

Trademarks

All trademarks used within this document are the property of their respective owners. VESA, DDC, E-DDC, DPMS, DPM, EDID, E-EDID, EVC, P&D, VDIF, GTF, CVT, VTB-EXT, DI-EXT and DisplayPort are trademarks of the Video Electronics Standards Association.

I^2C is a trademark owned by Philips.

Patents

VESA draws attention to the fact that it is claimed that compliance with this specification may involve the use of a patent or other intellectual property right (collectively, "*IPR*").. VESA takes no position concerning the evidence, validity, and scope of this *IPR*.

Attention is drawn to the possibility that some of the elements of this VESA *Specification* may be the subject of *IPR* other than any identified above. VESA shall not be held responsible for identifying any or all such *IPR*, and has made no inquiry into the possible existence of any such *IPR*.

THIS *SPECIFICATION* IS BEING OFFERED WITHOUT ANY WARRANTY WHATSOEVER, AND IN PARTICULAR, ANY WARRANTY OF NON-INFRINGEMENT IS EXPRESSLY DISCLAIMED. ANY IMPLEMENTATION OF THIS *SPECIFICATION* SHALL BE MADE ENTIRELY AT THE *IMPLEMENTER*'S OWN RISK, AND NEITHER VESA, NOR ANY OF ITS *MEMBERS* OR *SUBMITTERS*, SHALL HAVE ANY LIABILITY WHATSOEVER TO ANY *IMPLEMENTER* OR THIRD PARTY FOR ANY DAMAGES OF ANY NATURE WHATSOEVER DIRECTLY OR INDIRECTLY ARISING FROM THE IMPLEMENTATION OF THIS *SPECIFICATION*.

Support for this Standard

Clarifications and application notes to support this standard may be written. To obtain the latest standard and any support documentation, contact VESA.

If you have a product, which incorporates EDID, you should ask the company that manufactured your product for assistance. If you are a manufacturer, VESA can assist you with any clarification you may require. All comments or reported errors should be submitted in writing to VESA using one of the following methods.

- Fax: 510 651 5127, *direct this note to Technical Support at VESA*
- E-mail: support@vesa.org
- Mail: Technical Support
  Video Electronics Standards Association
  39899 Balentine Drive, Suite 125
  Newark, CA 94560

Conformance Glossary – Definition of Terms

The following is a list of definitions for certain keywords used through out this document:
shall: A keyword that indicates a mandatory requirement for compliance with this standard.
should: A keyword that indicates a choice with a strongly preferred preference – equivalent to "is strongly recommended".
may: A keyword that indicates a choice with no expressed or implied preference.
optional: A keyword that denotes items which may or may not be present in a complaint device.
required: A keyword that denotes items which are mandatory and shall be present in a compliant device.

Conformance Glossary – Definition of Notations

The following table defines a list of notations that are used through out this document:

Definitions of Notations

Notation	Definition	Example
-	Subtraction	7 – 3 = 4
÷	Division	9 ÷ 3 = 3
×	Multiplication	2 x 3 = 6
+	Addition	2 + 3 = 5
≡	Is Equivalent To	A ≡ B
→	Thru	7 → 3 ≡ 7, 6, 5, 4, 3
/	Delineator	Offset Pointer or Address
Binary	Binary Number, msb → lsb	(msb) 10010110 (lsb)
Hex	Hexadecimal Numbers, MSB → LSB	(MSB) 14 00 0A FF FEh (LSB)
Boldface Hex	Address or Offset	**3Fh** ≡ is an address located at **3Fh**
Hex Contents	Hex Contents at Address [__**h**]	[3Fh] ≡ the hex data stored at address **3Fh**
Bit Contents	Contents of Bits at Address [__**h**]	[Byte **7Ah**, bit 1, 0] ≡ Binary data stored in bits 1 & 0 at address **7Ah**
Dec String	String of Decimal Numbers	4, 3, 6, 4
Hex String	String of Hexadecimal Numbers	(14 00 0A FF FE)h

Revision History

Release A September 2, 1999

Initial release of the standard. The body of the standard is derived from the EDID Standard Ver. 3.0.

Release A Revision 1 February 9, 2000

Consolidate requirements of detailed timing section in section 3.10
Section 3.4 - removed restriction of 00h, 00h, 00h, 00h value for serial number field
Table 3.11 - added note to reference preferred timing mode bit requirements
Table 3.15 - added note for 1 : 1 AR (aspect ratio) in earlier EDID definitions
Table 3.16 – corrected order of bits in Vertical Sync format description
Table 3.17 - added definition for stereo flag bits values of 0,0,x
Table 3.20 - added clarification to round up Max pixel; clock value

Release A Revision 2 September 25, 2006

Preface - Added a Conformance Glossary for definitions of terms and notations.
Added a List of Tables.
Section 1 Overview - Revised Summary in Section 1.1 and added Scope in Section 1.2.
Section 1.5 Reference Documents - Revised list and partitioned into Section 1.5.1 Normative Documents and Section 1.5.2 Reference Documents.
Section 2 EDID Structures - Added Table 2.1 History of EDID Structures in Section 2.1; added Table 2.2 Comparison of EDID Structures (defines required, optional and recommended elements of EDID data structures 1.0 to 1.4) and added Section 2.1.7 Compatibility of EDID 1.x Structures.
Section 2.2 EDID Extension Blocks - Revised/added the following:
- Section 2.2.1 Order of EDID Extension Blocks - note that Block Maps are now optional;
- Section 2.2.2 General Extension Block Format;
- Section 2.2.3 EDID Block Map Extension and
- Section 2.2.4 EDID Extension Tags Assigned by VESA.

Section 3.1 EDID Format Overview - Updated contents of Table 3.1.
Section 3.4.1ID Manufacturer Name - Updated PNPID Contact Information.
Section 3.4.4 Week & Year of Manufacture - Added option to declare Model Year.
Section 3.6.1 Video Input Definition -Added Color Bit Depth declaration to Digital Video Interfaces and updated Supported Digital Interfaces.
Section 3.6.2 H & V Screen Size - Added option to declare Screen Aspect Ratio (Portrait or Landscape) in place of H & V Screen Size.
Section 3.6.4 Feature Support Byte - Added Supported Color Encoding Formats; Replaced Preferred Timing Mode (PTM) Bit with PTM includes or does not include Native Pixel Format/Preferred Refresh Rate of the display device and replaced GTF Bit with Continuous or Non-Continuous Frequency Display.
Section 3.10 - 18 Byte Descriptors - Changed terminology, formally known as Detailed Timing Descriptor Block.
Section 3.10.2 Detailed Timing Descriptor - Added option to include aspect ratio for DTV timing modes; included definitions for Analog Composite, Bipolar Analog Composite, Digital Composite & Digital Separate.
Section 3.10.3.3 Display Range Limits - formally known as Monitor Range Limits – increased range by adding optional Display Range Limits Offsets and added optional GTF (default), GTF (secondary curve) & CVT Support Information.
Section 3.10.3.7 Color Management Data - Added optional short hand CMD definition.

Section 3.10.3.8 3 Byte CVT Codes - Added optional 3 Byte CVT Codes.
Section 3.10.3.9 Established Timings III - Added optional Established Timings III.
Section 3.12 Notes Regarding Borders - Made corrections and updates to the video timing parameter definition drawing.
Section 4 EDID Extensions - Updates and corrections were added.
Section 5 Timing Information Priority Order - Updates and corrections were added.
Section 6 APPENDIX A – Three new sample EDID tables were included.
Section 7 APPENDIX B - Added GTF & CVT Compatibility Issues.
Section 8 APPENDIX C - Added a Glossary.
Section 9 APPENDIX D - Updated FAQ section.
Section 10 APPENDIX E - Added ASCII Reference Tables.

Acknowledgments

This document would not have been possible without the efforts of the VESA Display Systems Committee's EDID Task Group. In particular, the following individuals and their companies have contributed significant time and knowledge.

Release A, Rev. 2

Syed Athar Hussain	ATI Technologies	
Chi Tai Hong	Chrontel	
Joe Goodart	Dell	
James R. Webb	DisplayLabs	
Bob Myers	Hewlett-Packard	
Gang Han	NVIDIA	
Isaac Yang	NVIDIA	
Glenn Adler	Philips	
Ian Miller	Samsung	
Paul Doyle	Sony	
Robert Blanchard	Sony	
Joe Lamm	Tech Source	
Alain d'Hautecourt	ViewSonic	Task Group Chair & Editor

Release A, Rev. 1 and/or previous

Bill Milford	3Dfx
Warren Whaley	Canon
Joe Goodart	Dell
Drew Loucks	Elo Touchsystems
Bob Myers	Hewlett-Packard
Ton Wang	Hitachi
Ian Miller	IBM
Shaun Kerigan	IBM
En Anwyl	IBM
Geoff Gould	Intel
Rick Stoneking	Microchip Technology
Chuck Scott	Microsoft
Anthony Cianfarano	Mitsubishi
Jack Hosek	NEC
Richard Atanus	NEC
Anders Frisk	Nokia
Hans van der Ven	Panasonic
Glenn Adler	Philips
John Matsumoto	Toshiba
Alain d'Hautecourt	ViewSonic
Don Panell	

Table of Contents

Tables

1. OVERVIEW

1.1 Summary

The E-EDID Standard defines requirements and options for data structures that enable a display (sink) to inform the host (source) about its identity and capabilities. This standard also makes recommendations for some data fields. Host (source) devices are required to read and properly handle the data that a display (sink) provides with these data structures. The EDID data structure is independent of the communications protocol used between the display (sink) and the host (source). Enhanced EDID defines a basic data structure (known as BASE EDID or block 0) of 128 bytes that all compliant displays shall supply. E-EDID also defines the rules for how EXTENSIONS may be added to the BASE structure.

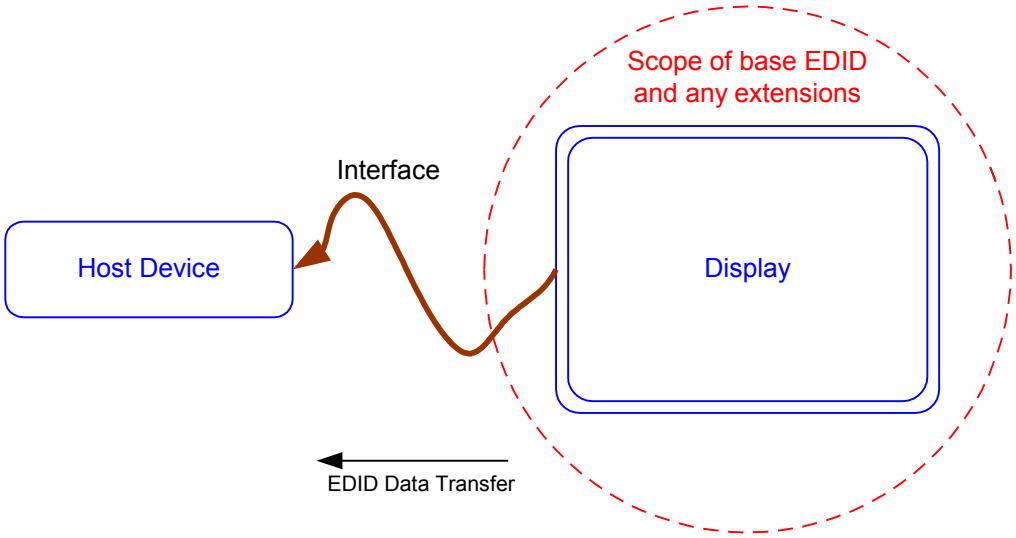
The Enhanced EDID family of documents:

1. Enhanced EDID Standard (Basic 128-byte data structure. Rules for how EDID EXTENSIONS are mapped.)
2. Optional EDID EXTENSION Standards (Definitions of the data structures contained in the optional EDID EXTENSIONS.) Refer to Section 2.2.4 of this standard for a list of current EDID EXTENSION Blocks. Contact the VESA office for the latest list of VESA and CEA defined EXTENSIONS.
3. VESA E-EDID Implementation Guide, Version 1.0, June 4, 2001.

1.2 Scope

The information contained within an EDID Structure, whether this is simply a BASE EDID or the combination of a BASE EDID and one or more EDID EXTENSIONS, relates to the whole display product and not individual elements of the product.

The drawing below shows this in graphical form – the BASE EDID (and any EDID EXTENSION) that is transferred from the display to the host device specifies capabilities of the combination of components and sub-assemblies contained within the display.



Note: Generally the display identified above will be a product connected to a host (source) via an external interface. However, in some cases products with an embedded display may use EDID, in which case the display above may be a subsystem of the product with an internal interface to the control (host) subsystem.

1.3 Background

Enhanced EDID was originally created to define how multiple optional EDID EXTENSIONS shall be attached to the BASE EDID. These EXTENSIONS shall be used to describe additional features and capabilities of current and future displays. This document also defines a revision (Version 1, Rev. 4) to the BASE EDID and shall supersede all previous versions of EDID. EDID structure Version 1, Rev. 4 is strongly recommended for all new designs.

1.4 Standard Objectives

The EDID Standard was developed by VESA to meet, exceed and/or complement certain criteria. These criteria are set forth as Standard Objectives as follows:

- Support VESA & Microsoft® Plug and Play definitions
- Provide information in a compact format to allow the graphics subsystem to be configured based on the capabilities of the attached display

1.5 Reference Documents

Note: Standards and document versions identified here are current (as of the release of this document), but users of this document are encouraged to ensure they have the latest versions of referenced standards and documents. These references have been separated into Normative Reference Documents and Informative Reference Documents.

1.5.1 NORMATIVE REFERENCE DOCUMENTS

Understanding the contents of the following normative reference documents is a requirement for understanding the provisions of this standard:

- ISO/IEC 8859-1: 1998 Information Technology - 8-bit single-byte coded graphic character sets - Part 1: Latin alphabet No. 1 -ASCII Codes
- VESA Coordinated Video Timing (CVT™) Standard, Version 1.1, September 10, 2003
- VESA Display Color Management (DCM™) Standard, Version 1, January 6, 2003
- VESA Display Information Extension (DI-EXT™) Block Standard, Release A, August 21, 2001
- VESA Display Power Management (DPM™) Standard, Release A, March 3, 2003
- VESA Enhanced Display Data Channel Standard (E-DDC™), Version 1, September 2, 1999
- VESA and Industry Standards and Guidelines for Computer Display Monitor Timing (DMT™), Version 1.0, Revision 10, October 29, 2004
- VESA Plug & Play (PnP™) Standard for the Display/Graphics Subsystem, Release A, June 7, 2004
- CIE 15.2 Colorimetry Revision 86, Date: 1986

1.5.2 INFORMATIVE REFERENCE DOCUMENTS

The following informative reference documents contain information that is useful in understanding this standard:

- DVI Specifications, Revision 1.0, 02 April 1999 - www.ddwg.org
- CEA-861-D Standard, A DTV Profile for Uncompressed High Speed Digital Interfaces; www.global.ihs.com
- HDMI Specifications: Refer to www.hdmi.org for more information on HDMI.
- Microsoft Windows and the Plug and Play Framework Architecture, March 1994,
- Microsoft Plug and Play for Windows 2000 and Windows XP, December 2001,
- Microsoft Windows XP – Plug and Play Overview…
- Microsoft Plug and Play Technology, December 2001.

- Microsoft - Windows Vista Logo Program Client System Requirements, Version 3.0, Draft Revision 0.9 - www.microsoft.com/whdc/winlogo/hwrequirements.mspx
- VESA Enhanced EDID Localized String Extension (LS-EXT™) Standard, Release A, July 10, 2003
- VESA E-EDID Implementation Guide, Version 1.0, June 4, 2001
- VESA Generalized Timing Formula Standard (GTF™), Version 1.0, December 18, 1996
- VESA Video Timing Block Extension (VTB-EXT™) Data Standard, Release A, Nov. 24, 2003
- VESA Video BIOS Extensions for Display Data Channel Standard - VBE/DDC™, Version 1.1, Nov. 18, 1999
- VESA Glossary of Terms: Go to www.vesa.org and click on Glossary of Term for access to an interactive online glossary.

2. EDID STRUCTURES

2.1 BASE EDID: Past and Present

Table 2.1 shows the history of EDID Structure definitions:

Table 2.1 - EDID Structures – History

Standard	Version / Release	Revision	Date	Base EDID Structure(s)	Comment
DDC	V1.0	0	8/12/94	V1 R0	128 bytes – initial definition
EDID	V2	0	4/09/96	V1 R0	128 bytes - permitted, no definition
				V1 R1	128 bytes – revised definition based on V1 R0
EDID	V2	1	7/24/96	V1 R0	128 bytes - permitted, no definition
				V1 R1	128 bytes – preferred definition
EDID	V3	-	11/13/97	V1 R0	128 bytes - permitted, no definition
				V1 R1	128 bytes - permitted, no definition
				V1 R2	128 bytes – revised definition based on V1 R1
				V2 R0	256 bytes for P&D standard – new definition
E-EDID	Release A	-	9/02/99	V1 R0	128 bytes, use to end 1/1/2000 – no definition
				V1 R1	128 bytes, use to end 1/1/2000 – no definition
				V1 R2	128 bytes, use to end 1/1/2000 – no definition
				V1 R3	128 bytes - revised definition based on V1 R2
				V2 R0	256 bytes for P&D standard - permitted, no definition
E-EDID	Release A	1	2/09/00	V1 R3	128 bytes – preferred definition
				V2 R0	256 bytes for P&D standard - permitted, no definition
E-EDID	Release A	2P	TBD	V1 R4	128 bytes – revised definition based on V1 R3

The following sections (2.1.1 → 2.1.5) provide additional information on the history of EDID 1.x structure definitions.

2.1.1 EDID 1.0

EDID structure 1.0 (Version 1, Revision 0) was the original 128-byte file format introduced in the DDC Standard Version 1.0 Revision 0 issued in August 1994. EDID 1.0 shall not be used in new display products.

2.1.2 EDID 1.1

EDID structure 1.1 added definitions for monitor descriptors as an alternate use of the space originally reserved for detailed timings, as well as definitions for previously unused fields. Structure 1.1 was introduced in the EDID Standard Version 2 issued in April 1996. EDID 1.1 shall not be used in new display products.

2.1.3 EDID 1.2

EDID structure 1.2 added definitions to existing data fields. Structure 1.2 was introduced in EDID Standard Version 3. EDID 1.2 shall not be used in new display products.

2.1.4 EDID 1.3

EDID structure 1.3 added definitions for secondary Generalized Timing Formula (GTF) curve coefficients. Structure 1.3 was introduced in E-EDID Standard Release A issued in September 1999. EDID 1.3 was based on the same core as all other EDID 1.x structures.

Structure 1.3 is a superset of structure 1.2. The main difference between the two is that 1.3 allows the Monitor Range Limits descriptor to define coefficients for a secondary GTF curve, and mandates a certain set of monitor descriptors. EDID 1.3 is strongly discouraged for use in new display product designs.

2.1.5 EDID 1.4

EDID structure 1.4 is introduced in this document. EDID structure 1.4 adds support for Consumer Electronic Products (Model Year and Aspect Ratio) and PC Products (CVT, Established Timings III, Additional Video Interfaces, Expanded Display Range Limits, optional Product Features and Timing Mode Priorities). Certain Display Descriptors (formally known as Monitor Descriptors) that were mandatory in EDID 1.3 are now optional.

EDID 1.4 is based on the same core as all other EDID 1.x structures. EDID 1.4 is the new baseline for EDID data structures and is strongly recommended for all new designs. However, there are a few incompatible data fields in EDID 1.4 that were changed to support emerging industry requirements.

Structure 1.4 is a superset of structure 1.3. The main difference between the two is that 1.4 allows the Display Range Limits descriptor to define support for CVT, and certain display descriptors mandated in EDID 1.3 are now optional. Some additional changes have been included to provide support for DTV products.

2.1.6 EDID Structures --- Comparison Table

Table 2.2 contains a comparison of EDID Data Structures (1.0 through 1.4). The table contains a listing of required, optional and optional (but recommended) ELEMENTS. Refer to the Key in Table 2.3 for the definitions of the symbols used in the Table 2.2.

Table 2.2 - EDID Structures – Comparison Table

	BASE EDID Structure				
	1.0	**1.1**	**1.2**	**1.3**	**1.4**
Block "0" Header	☺	☺	☺	☺	☑
ID Manufacturer	☺	☺	☺	☺	☑
ID Product Code	☺	☺	☺	☺	☑
ID Serial Number	☒	☒	☒	☒	☒
Week of Manufacture	☒	☒	☒	☒	☒
Year of Manufacture or Model Year	☺	☺	☺	☺	☑
EDID version	☑	☑	☑	☑	☑
EDID revision	☑	☑	☑	☑	☑
Basic Display Parameters & Features	☺	☺	☺	☺	☑
Display x, y Chromaticity Coordinates (Phosphor or Filter Chromaticity)	☺	☺	☺	☺	☑
Established Timings	☒	☒	☒	☒	☒
Standard Timing Identifications	☒	☒	☒	☒	☒
Preferred Timing Descriptor Block	☒	☒	☒	☑	☑
Range Limits Descriptor Block	n/a	☒	☒	☑	☯
Monitor Name Descriptor Block	n/a	☒	☒	☑	☯
Other Descriptor Blocks	n/a	☒	☒	☒	☒
Extension flag	☺	☺	☺	☺	☑
Checksum	☺	☺	☺	☺	☑

Table 2.3 - EDID Structures – Comparison Table - Key

☑	Explicit requirement --- mandatory (a "shall")
☺	No requirement stated but commonly understood to be a requirement
☯	Optional but recommended
☒	Optional
n/a	Not applicable

2.1.7 Compatibility of EDID 1.x Data Structures --- Handling Updates to EDID Data Structures

On occasion, VESA will publish updates (revisions) to the E-EDID Standard. Some of these updated standards may contain new EDID structure definitions. When VESA publishes a new EDID structure with a new revision number (and the version number stays the same), the new EDID structure is backward compatible (key ELEMENTS only). For legacy support, an older host system (that recognizes EDID version 1, revision 3, for example) connected to a display product with a newer EDID structure (for example; version 1, revision 4), the host shall decode the EDID data using the older EDID structure definitions (for example; version 1, revision 3 definitions).

When doing this, the host (graphics system driver or operating system) EDID read and decode may result in some errors. The host (graphics system driver or operating system) may not understand certain ELEMENTS or data fields within the EDID Block. The host shall ignore these ELEMENTS or data fields. The "Plug & Play" process must still work.

If an internet connection is available, the older host may search for a driver that can decode the newer EDID structure.

An older host (source) shall never shut down a connected video output port when it detects a display with a newer EDID structure which the host may not completely understand. For more information on this subject, refer to the VESA PnP Standard or appropriate standard or document for the interface or application in question.

2.2 EDID EXTENSION Blocks

E-EDID, based on EDID structure 1.4, allows additional data to be stored using multiple (one or more) EXTENSION Blocks attached to BASE EDID in a single file. In the minimum configuration, E-EDID consists of just one data Block --- the BASE EDID, also known as Block 0. Each Block is 128 bytes in length.

2.2.1 EDID EXTENSIONS: Order of the Blocks

EXTENSION Blocks are arranged sequentially after Block 0. BASE EDID is stored in Block 0 and is the only mandatory Block. Table 2.4 describes the Enhanced EDID high level layout of the required BASE EDID Block and optional EXTENSION Blocks.

Table 2.4 – E-EDID High Level Layout

Segment Pointer / Addresses	Block Number 'N'	EDID 1.3 Block Description	EDID 1.4 Block Description
00h / 00h → 7Fh	0	BASE EDID 1.3 Structure	BASE EDID 1.4 Structure
00h / 80h → FFh	1	EXTENSION Block 1 if N = 1 or Block Map 1 if $2 \leq N \leq 127$	EXTENSION Block 1 or Block Map 1 (Optional)
01h / 00h → 7Fh	2	EXTENSION Block 2	EXTENSION Block 2
01h / 80h → FFh	3	EXTENSION Block 3	EXTENSION Block 3
02h / 00h → 7Fh	4	EXTENSION Block 4	EXTENSION Block 4
●●h / 00h → 7Fh	●●●	EXTENSION Block ●●●	EXTENSION Block ●●●
●●●	●●●	●●●	●●●
3Fh / 80h → FFh	127	EXTENSION Block 127	EXTENSION Block 127
40h / 00h → 7Fh	128	Block Map 2 if $129 \leq N \leq 254$	Block Map 2 (Optional) or EXTENSION Block 128
40h / 80h → FFh	129	EXTENSION Block 129	EXTENSION Block 129
●●h / 00h → 7Fh	●●●	EXTENSION Block ●●●	EXTENSION Block ●●●
●●●	●●●	●●●	●●●
7Eh / 80h → FFh	253	EXTENSION Block 253	EXTENSION Block 253
7Fh / 00h → 7Fh	254	EXTENSION Block 254	EXTENSION Block 254
7Fh / 80h → FFh	255	Block 255 is not available.	If Block Maps are not used then Block 255 is an EXTENSION Block. If Block Maps are used then Block 255 is not available.

Notes to Table 2.4:

1. Refer to VESA's E-DDC Standard for more information on the Segment Pointer and Addresses shown in Table 2.4.
2. For EDID 1.3, if the maximum value of N is '1', then Block 1 contains an Extension Block as defined in sections 2.2.2 and 2.2.4. If the maximum value of N is more than or equal to '2' and less than or equal to '127', then Block 1 is Block Map 1. If the maximum value of N is more than or equal to '129' and less than or equal to '254', then Block 128 is Block Map 2. Block Maps are considered to be EXTENSION Blocks to the base EDID and shall be included in the EXTENSION Block Flag at address **7Eh** in the Base EDID (Block 0).
3. For EDID 1.4, Block Maps are optional. Blocks 1 and 128 may contain optional Extension Blocks as defined in sections 2.2.3 and 2.2.4 or they may contain Block Maps.
4. All Blocks shall be sequentially stored with no gaps or empty Blocks.
5. A partial list of defined Extension Blocks is shown in Table 2.7.
6. The variable 'N' in table 2.4 contains the total number of EXTENSION Blocks listed at address 7Eh of the BASE EDID (Block 0). This includes Block Map/s when present.

2.2.2 EDID Extensions: General Extension Block Format

Several EXTENSION Blocks have already been defined to contain specific kinds of data. Refer to section 2.2.4 for a list of EXTENSION Blocks. All EXTENSION Blocks except the EXTENSION Block Map shall include one byte for the EXTENSION Block revision number.

Table 2.5 - EDID Structure – General Extension Block Format

Address	Byte #	Value	Description
00h	0	Refer to section 2.2.4	EXTENSION Block Tag Number
01h	1	00h → FFh	Revision number for this EXTENSION Block. One byte binary number. Revisions shall be backward compatible (partial).
		Block Tag Number	Exception: EXTENSION Block Map --- EXTENSION Blocks 1 & 128
02h → 7Eh	2 → 126	00h → FFh	EXTENSION Block Data
		Block Tag Number	Exception: EXTENSION Block Map --- EXTENSION Blocks 1 & 128
7Fh	127	00h → FFh	Checksum for this EXTENSION Block

2.2.3 EDID Extensions: EDID Block Map Extension

The EXTENSION Block Map (in EXTENSION Blocks #1 & #128) is an optional ELEMENT for EDID structure (Version 1, Revision 4). The EXTENSION Block Map (in EXTENSION Blocks #1 & #128) is a required ELEMENT for EDID structure (Version 1, Revision 3).
An EXTENSION Block map is a special EXTENSION Block that lists tag numbers for all EXTENSION Blocks are stored in a particular display's EDID memory. The tag number entries of the EXTENSION Block Map, prepared by the display manufacturer, shall match the tag numbers of all EXTENSION Blocks that are stored in a display's memory. For a partial listing of EXTENSION Block Tag Numbers refer to Section 2.2.4.

Table 2.6 - EDID Structure – Block Map Extension

Address	Byte #	Value	Description
00h	0	F0h	EXTENSION Block Tag Number designates "EXTENSION Block Map"
01h	1	Block Tag Number	EXTENSION Block Tag Number for the data stored in EXTENSION block 2 or block 129
02h	2	Block Tag Number	EXTENSION Block Tag Number for the data stored in EXTENSION block 3 or block 130
●●●	●●●	●●●	●●●
●●●	●●●	●●●	●●●
●●●	●●●	●●●	●●●
7Eh	126	Block Tag Number	EXTENSION Block Tag Number for the data stored in EXTENSION block 127 or block 254
7Fh	127	00h → FFh	Checksum for this EXTENSION Block Map

Notes to Table 2.6:

1. A partial list of assigned EXTENSION Block Tag Numbers is listed in Section 2.2.4. Contact the VESA Office for the latest list of EXTENSION Block Tag Numbers.
2. All EXTENSION Block Tag Numbers shall be sequentially listed (in the Block Map EXTENSION) in the order that the EXTENSION Blocks are stored in EDID memory.
   Addresses without Block Tag Numbers shall be padded with '00h'.

2.2.4 EDID Extension Tags Assigned by VESA

EXTENSION Block Tag Numbers are used to numerically identify each type of EXTENSION Block. VESA and other standards groups have developed, and continue to develop, useful EDID EXTENSION Block Standards. VESA maintains the master list of assigned EDID EXTENSION Block Tag Numbers.

Table 2.7 - EDID Structure – Extension Tag Numbers

Tag Numbers	Extension Block Description
02h	CEA-EXT: CEA 861 Series Extension (see Note 2)
10h	VTB-EXT: Video Timing Block Extension
40h	DI-EXT: Display Information Extension
50h	LS-EXT: Localized String Extension
60h	DPVL-EXT: Digital Packet Video Link Extension
F0h	EXTENSION Block Map
FFh	EXTENSIONS defined by the display manufacturer

Notes to Table 2.7:

1. Contact the VESA office for the latest list of published EDID EXTENSIONS.
2. Refer to the latest revision of the CEA 861 Standard.
3. The EXTENSION Block Maps (Tag F0h) located at block 1 and block 128 are in themselves EXTENSION Blocks and shall be included in the Number of EXTENSION Blocks listed at address **7Eh** in the base EDID (block 0).
4. More than one copy of the extension blocks (in Table 2.7) may be included in an EDID structure. However, the Block Map EXTENSION (Tag F0h) is limited to 1 or 2 blocks.

3. Extended Display Identification Data (EDID) Version 1 Revision 4

3.1 EDID Format Overview

Table 3.1 - EDID Structure Version 1, Revision 4

Address	Bytes	Description	Format
00h	**8**	**Header:** = (00 FF FF FF FF FF FF 00)h	See Section 3.3
08h	**10**	**Vendor & Product Identification:**	See Section 3.4
08h	2	ID Manufacturer Name	ISA 3-character ID Code
0Ah	2	ID Product Code	Vendor assigned code
0Ch	4	ID Serial Number	32-bit serial number
10h	1	Week of Manufacture	Week number or Model Year Flag
11h	1	Year of Manufacture or Model Year	Manufacture Year or Model Year
12h	**2**	**EDID Structure Version & Revision:**	See Section 3.5
12h	1	Version Number: = 01h	Binary
13h	1	Revision Number: = 04h	Binary
14h	**5**	**Basic Display Parameters & Features:**	See Section 3.6
14h	1	Video Input Definition	See Section 3.6.1
15h	1	Horizontal Screen Size or Aspect Ratio	Listed in cm. → Aspect Ratio --- Landscape
16h	1	Vertical Screen Size or Aspect Ratio	Listed in cm. → Aspect Ratio --- Portrait
17h	1	Display Transfer Characteristic (Gamma)	Binary --- Factory Default Value
18h	1	Feature Support	See Section 3.6.4
19h	**10**	**Color Characteristics:**	See Section 3.7
19h	1	Red/Green: Low Order Bits	Rx1 Rx0 Ry1 Ry0 Gx1 Gx0 Gy1Gy0
1Ah	1	Blue/White: Low Order Bits	Bx1 Bx0 By1 By0 Wx1 Wx0 Wy1 Wy0
1Bh	1	Red-x: High Order Bits	Red-x Bits 9 → 2
1Ch	1	Red-y: High Order Bits	Red-y Bits 9 → 2
1Dh	1	Green-x: High Order Bits	Green-x Bits 9 → 2
1Eh	1	Green-y: High Order Bits	Green-y Bits 9 → 2
1Fh	1	Blue-x: High Order Bits	Blue-x Bits 9 → 2
20h	1	Blue-y: High Order Bits	Blue-y Bits 9 → 2
21h	1	White-x: High Order Bits	White-x Bits 9 → 2
22h	1	White-y: High Order Bits	White-y Bits 9 → 2
23h	**3**	**Established Timings**	See Section 3.8
23h	1	Established Timings I	
24h	1	Established Timings II	
25h	1	Manufacturer's Reserved Timings	
26h	**16**	**Standard Timings: Identification 1 → 8**	See Section 3.9
36h	**72**	**18 Byte Data Blocks**	See Section 3.10
36h	18	Preferred Timing Mode	
48h	18	Detailed Timing # 2 or Display Descriptor	
5Ah	18	Detailed Timing # 3 or Display Descriptor	
6Ch	18	Detailed Timing # 4 or Display Descriptor	

7Eh	**1**	**Extension Block Count N**
		If Block Maps are used then
		00h ≤ N ≤ FEh and FFh is invalid.
		If Block Maps are not used then
		00h ≤ N ≤ FFh.
			Number of (optional) 128-byte EDID EXTENSION blocks to follow – if Block Maps are used then 254 is the maximum value of 'N'. If Block Maps are not used then 255 is the maximum value of 'N'.

7Fh	**1**	**Checksum C** 00h ≤ C ≤ FFh	The 1-byte sum of all 128 bytes in this EDID block shall equal zero

Notes for Table 3.1:

1. Table 3.1 is for reference only. Refer to the appropriate sections (3.3 to 3.11) for the definitions of the various data fields within BASE EDID.
2. If there are two or more EXTENSION Blocks, then the number of EXTENSION Blocks listed at address **7Eh** shall also include the optional EDID Block Map EXTENSION (if present). The EDID Block Map EXTENSION is an EXTENSION Block to the BASE (Block 0) EDID structure. For example, if there are two EDID EXTENSION Data Blocks, then add the EDID Block Map EXTENSION and enter the number three at address **7Eh**.
3. EDID structure Version 1, Revisions 1 and 2, allowed the First 18 Byte Data Block to be used for Monitor Descriptors. Host SW using this data should be prepared to detect Monitor Descriptors also in this location even though displays conforming with later revisions (1.3 & 1.4) of EDID structure only use this space for the Preferred Timing Mode (a Detailed Timing Description). For EDID 1.4, the term Monitor Descriptors has been replaced with the term Display Descriptors.

3.2 Data Format Conventions

The EDID structures are designed to be compact in their representation of data fitting the most information into a limited space. To accommodate this, many data lengths have been used according to the needs of the particular data. These include fields from a single bit up to several bytes in length. In all cases, except where explicitly stated, the following conventions shall be used:

Table 3.2 - Data Format Conventions

Data length	Convention used	Example
1 to 7 bits	stored in stated order	
8 bits (1 byte)	stored at stated location	
9 to 15 bits	location of bits stated in field definition	
16 bits (2 bytes)	Bytes are stored as binary (not BCD) in specified locations. The least significant byte (LSB) is stored in the first location.	1280 decimal = 0500h Stored as 00h in first location and 05h in the next location
Character string (More than 2 bytes)	Bytes are stored as ASCII, in the order they appear in the string.	"ACED" Stored as 41h in first location, 43h in the next location, 45h in the next location and 44h in the last location.

The following sections (3.3 to 3.11) provide details on each byte of the EDID 1.4 data structure.

3.3 Header: 8 Bytes

The header is an 8-byte pattern designed to be easily recognizable from other bytes in the data structure. The header is a required ELEMENT in EDID data structure version 1.4. Its format is shown in Table 3.3.

Table 3.3 - EDID Header Format

Address	8 Bytes	Value
00h	1	00h
01h	1	FFh
02h	1	FFh
03h	1	FFh
04h	1	FFh
05h	1	FFh
06h	1	FFh
07h	1	00h

3.4 Vendor & Product ID: 10 Bytes

The vendor & product ID block is made up of several data fields used to uniquely identify the display product. The size and order of each field is shown in the Table 3.4.

Table 3.4 – Vendor & Product ID Structure

Addresses	10 Bytes	Vendor & Product Identification	Refer To
08h, 09h	2	ID Manufacturer Name	Section 3.4.1
0Ah, 0Bh	2	ID Product Code	Section 3.4.2
0Ch → 0Fh	4	ID Serial Number	Section 3.4.3
10h, 11h	2	Week of Manufacture or Model Year Flag, Year of Manufacture or Model Year	Section 3.4.4

3.4.1 ID Manufacturer Name: 2 Bytes

The ID manufacturer name field is a required ELEMENT in EDID structure 1.4. The ID manufacturer name field, shown in Table 3.5, contains a 2-byte representation of the display manufacturer's 3 character code. These codes are also called the ISA (Industry Standard Architecture) Plug and Play Device Identifier (PNPID). They are based on 5 bit compressed ASCII codes; for example: "00001=A" ... "11010=Z".

ISA Manufacturer PNPIDs are issued by Microsoft. Contact Microsoft by email, fax or website:

E-mail: PnPID@Microsoft.com.
Fax: 425-936-7329, Attention PNPID in Building 27.
URL: Refer to http://www.microsoft.com/whdc/system/pnppwr/pnp/pnpid.mspx for more information on ISA PNPID.

Table 3.5 - ID Manufacturer Name

Address	Byte #	Bits at Address 08h	Bits at Address 09h	Description
08h	1	**7** 0 1		**Bit 7 is reserved** Set bit 7 to 0 Reserved – Do Not Use
		6 5 4 3 2 0 4 3 2 1 0		**Character #1 Location** Compressed ASCII Code - Bit #
08h/09h	1 & 2	**1 0** 0 4 3	**7 6 5** 2 1 0	**Character #2 Location** Compressed ASCII Code - Bit #
09h	2	0	**4 3 2 1 0** 4 3 2 1 0	**Character #3 Location** Compressed ASCII Code - Bit #

3.4.2 ID Product Code: 2 Bytes

The ID product code field is a required ELEMENT in EDID structure version 1, revision 4. The ID product code field, shown in Table 3.6, contains a 2-byte manufacturer assigned product code. This is used to differentiate between different models from the same manufacturer, for example a model number. The 2 byte number is stored in hex with the least significant byte listed first.

Table 3.6 – ID Product Code

Address	2 Bytes	Value	Description
0Ah	1	00h → FFh	ID Product Code - LSB
0Bh	1	00h → FFh	ID Product Code - MSB

3.4.3 ID Serial Number: 4 Bytes

The ID serial number is a 32-bit serial number used to differentiate between individual instances of the same display model. Its use is optional. When used, the bit order for this field shall follow that shown in Table 3.7. The four bytes of the serial number are listed least significant byte (LSB) first. The range of this serial number is 0 to 4,294,967,295. This serial number is a number only --- it shall not represent ASCII codes. If this field is not used, then enter "00h, 00h, 00h, 00h".

Table 3.7 - ID Serial Number

Address	Byte #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Description
0Ch	1	(7	6	5	4	3	2	1	0)	ID Serial Number
0Dh	2	(15	14	13	12	11	10	9	8)	
0Eh	3	(23	22	21	20	19	18	17	16)	
0Fh	4	(31	30	29	28	27	26	25	24)	

Note for Table 3.7: The EDID structure version 1, revision 1 (and newer) offers a way to represent the serial number of the monitor as an ASCII string in a separate descriptor block. Refer to section 3.10.3 Display Descriptors for an alternative method of defining a serial number.

3.4.4 Week and Year of Manufacture or Model Year: 2 Bytes

There are two definitions for this data field: Week & Year of Manufacture or Model Year.

The week of manufacture field is optional, but the year of manufacture (or model year) field is required in EDID structure 1.4. The week of manufacture field (if used) is set to a value in the range of 1-54 weeks. If the week of manufacture field is not used, the value shall be set to '00h'.
The year of manufacture field is used to represent the year of the display's manufacture or the model year. If the year of manufacture field is used to represent the model year, then set the week of manufacture (at address **10h**) to 'FFh'. Then enter the model year (at address **11h**). The value that is stored is an offset from the year 1990 as derived from the following equation:

Stored Value = (Year of Manufacture {or Model Year} - 1990)

Table 3.8 – Week & Year of Manufacture or Model Year

Address	2 Bytes	Value	Description
10h	1	00h	Week of Manufacture is not specified
		01h → 36h	Week of Manufacture is specified (range is 1 → 54 weeks)
		37h → FEh	Reserved: Do not use
		FFh	Model Year Flag --- Model Year is specified at address **11h**
11h	1	00h → 0Fh	Reserved: Do not use
		10h → FFh	If Byte **10h** = FFh then Byte **11h** contains Model Year
		10h → FFh	If Byte **10h** ≠ FFh then Byte **11h** contains Year of Manufacture

Example 1: For a display manufactured in the first week of 2006, the values stored in these fields are 1 decimal (01h) at address **10h** and 16 decimal (10h) at address **11h**.

Example 2: Model year (2006) is indicated by storing FFh and 10h at addresses **10h** and **11h**, respectively.

3.5 EDID Structure Version & Revision: 2 Bytes

The EDID structure version number and revision number fields are required ELEMENTS in EDID structure version 1, revision 4. Version 1, revision 4 shall be stored here. These values define the EDID data structure being used. Display products compliant with this standard shall have Version Number = 1 and Revision Number = 4.

Table 3.9 - EDID Structure Version and Revision Numbers

Address	2 Bytes	Value	Description
12h	1	01h	EDID Structure Version Number 1
		00h, 02h → FFh	Reserved: Do not use
13h	1	04h	EDID Structure Revision Number 4
		00h → 03h, 05h → FFh	Reserved: Do not use

Note: Values < '04h' in address **13h** represent an earlier (and are superseded) revision number.

3.6 Basic Display Parameters and Features: 5 Bytes

The basic display parameters and features fields are required ELEMENTS in EDID data structure version 1, revision 4. The contents of the Basic Display Parameters and Features data fields are listed in Table 3.10.

Table 3.10 - Basic Display Parameters and Features

Address	5 Bytes	Basic Display Parameters & Features	Refer To
14h	1	Video Input Definition	Section 3.6.1
15h, 16h	2	Horizontal Screen Size or Aspect Ratio 'Landscape' Vertical Screen Size or Aspect Ratio 'Portrait'	Section 3.6.2
17h	1	Display Transfer Characteristic (Gamma)	Section 3.6.3
18h	1	Feature Support	Section 3.6.4

3.6.1 Video Input Definition: 1 Byte

The video input definition field is a required ELEMENT in EDID data structure version 1, revision 4. The host (source) shall use the information contained within the video input definition field to configure the video output of the host (source). The format of this one-byte field is described below in Table 3.11

Table 3.11 - Video Input Definition

Address	Bit Definitions								Description	
14h	**7**	_	_	_	_	_	_	_	**Video Signal Interface:**	Bit 7
	0								Input is an Analog Video Signal Interface:	
	7	**6**	**5**						**Signal Level Standard:** Video : Sync : Total	Bits 6 & 5
	0	0	0	_	_	_	_	_	0.700 : 0.300 : 1.000 V p-p	
	0	0	1	_	_	_	_	_	0.714 : 0.286 : 1.000 V p-p	
	0	1	0	_	_	_	_	_	1.000 : 0.400 : 1.400 V p-p	
	0	1	1	_	_	_	_	_	0.700 : 0.000 : 0.700 V p-p	
	7	_	_	**4**	_	_	_	_	**Video Setup:**	Bit 4
	0	_	_	0	_	_	_	_	Video Setup: Blank Level = Black Level	
	0	_	_	1	_	_	_	_	Video Setup: Blank-to-Black setup or pedestal	(see Note 1)
	7	_	_	_	**3**	**2**	**1**	_	**Synchronization Types:**	Bits 3 → 1
	0	_	_	_	0	_	_	_	Separate Sync H & V Signals are not supported	
	0	_	_	_	1	_	_	_	Separate Sync H & V Signals are supported	
	0	_	_	_	_	0	_	_	Composite Sync Signal on Horizontal is not supported	
	0	_	_	_	_	1	_	_	Composite Sync Signal on Horizontal is supported	
	0	_	_	_	_	_	0	_	Composite Sync Signal on Green Video is not supported	
	0	_	_	_	_	_	1	_	Composite Sync Signal on Green Video is supported	
	7	_	_	_	_	_	_	**0**	**Serrations:**	Bit 0
	0	_	_	_	_	_	_	0	Serration on the Vertical Sync is not supported	
	0	_	_	_	_	_	_	1	Serration on the Vertical Sync is supported	(see Note 2)
14h	**7**	_	_	_	_	_	_	_	**Video Signal Interface:**	Bit 7
	1								Input is a Digital Video Signal Interface:	(see Note 3)
	7	**6**	**5**	**4**	_	_	_	_	**Color Bit Depth:**	Bits 6 → 4
	1	0	0	0	_	_	_	_	Color Bit Depth is undefined	
	1	0	0	1	_	_	_	_	6 Bits per Primary Color	
	1	0	1	0	_	_	_	_	8 Bits per Primary Color	
	1	0	1	1	_	_	_	_	10 Bits per Primary Color	
	1	1	0	0	_	_	_	_	12 Bits per Primary Color	
	1	1	0	1	_	_	_	_	14 Bits per Primary Color	
	1	1	1	0	_	_	_	_	16 Bits per Primary Color	
	1	1	1	1	_	_	_	_	Reserved (Do Not Use)	
	7	_	_	_	**3**	**2**	**1**	**0**	**Digital Video Interface Standard Supported:**	Bits 3 → 0
	1	_	_	_	0	0	0	0	Digital Interface is not defined	(see Note 4)
	1	_	_	_	0	0	0	1	DVI is supported	
	1	_	_	_	0	0	1	0	HDMI-a is supported	
	1	_	_	_	0	0	1	1	HDMI-b is supported	
	1	_	_	_	0	1	0	0	MDDI is supported	
	1	_	_	_	0	1	0	1	DisplayPort is supported	
	1	_	_	_	→	→	→	→	All remaining values for Bits 3 → 0 are Reserved: Do Not Use	

Notes to Table 3.11:

1. Refer to the appropriate analog video signal level standard for the correct blank-to-black setup level or pedestal amplitude.
2. Serrations of the Vertical Sync Pulse are required when composite sync or sync-on-green video is used.
3. For EDID 1.4, if bit 7 (at address **14h**) is set to '1', then bits 4 & 3 (at address **18h**) define the Supported Color Encoding Format/s (refer to Table 3.14).
4. For more information, refer to the appropriate Digital Video Interface Standard.
5. If a display supports more than one synchronization type, then separate sync H & V signals have the highest priority and composite sync signals on horizontal have the lowest priority.

3.6.2 Horizontal and Vertical Screen Size or Aspect Ratio: 2 Bytes

The horizontal and vertical screen size or aspect ratio parameter fields are required ELEMENTS in EDID structure version 1, revision 4 for all display products except for certain types of projectors. The horizontal and vertical screen size parameters provide information on the screen dimensions of the display device, rounded to the nearest centimeter (cm). These 2 bytes may also be defined as aspect ratio in the 'Landscape' or 'Portrait' screen orientation mode - see Table 3.12. Aspect ratios are rounded to the hundredth decimal place.
The host (source) is expected to use this data to get a rough idea of the image size to generate properly scaled text and icons.
Use the following equations when determining the stored value (in Table 3.12) for the aspect ratio:

Landscape Orientation:
Given the Stored Value, the Aspect Ratio may be calculated by using the following equation:

$$\text{Aspect Ratio} = (\text{Stored Value} + 99) \div 100$$

Given the Aspect Ratio, the Stored Value may be calculated by using the following equation:

$$\text{Stored Value} = (\text{Aspect Ratio} \times 100) - 99$$

Portrait Orientation:
Given the Stored Value, the Aspect Ratio may be calculated by using the following equation:

$$\text{Aspect Ratio} = 100 \div (\text{Stored Value} + 99)$$

Given the Aspect Ratio, the Stored Value may be calculated by using the following equation:

$$\text{Stored Value} = (100 \div \text{Aspect Ratio}) - 99$$

Table 3.12 - Horizontal and Vertical Screen Size or Aspect Ratio

Address	2 Bytes	Value	Description
15h	1	01h → FFh	If byte **16h** ≠ 00h then byte **15h** = Horizontal Screen Size in cm. (Range is 1 cm → 255 cm)
		01h → FFh	If byte **16h** = 00h then byte **15h** = Aspect Ratio (Landscape) (Range is 1 : 1 AR → 3.54 : 1 AR)
		00h	If byte **15h** = 00h then byte **16h** = Aspect Ratio (Portrait)
16h	1	01h → FFh	If byte **15h** ≠ 00h then byte **16h** = Vertical Screen Size in cm. (Range is 1 cm → 255 cm)
		01h → FFh	If byte **15h** = 00h then byte **16h** = Aspect Ratio (Portrait) (Range is 0.28 : 1 AR → 0.99 : 1 AR)
		00h	If byte **16h** = 00h then byte **15h** = Aspect Ratio (Landscape)
15h, 16h	2	00h, 00h	If both bytes **15h** and **16h** = 00h then the screen size or aspect ratio are unknown or undefined.

Notes on Table 3.12:

1. The screen size bytes at addresses **15h** and **16h** shall be set to '00h', when the display manufacturer does not, or cannot specify the display's screen size. For example: A front projection display (with zoom feature) for example, may have an image of indeterminate size and the screen size bytes shall be set to 00h, 00h.
2. For displays that pivot, the screen size is measured in the landscape mode (major axis is on the horizontal, minor axis is on the vertical). This applies to displays that have the following aspect ratios: 4 : 3 AR, 5 : 4 AR, 15 : 9 AR, 16 : 9 AR and 16 : 10 AR.

3. Examples:

3-1. Landscape Orientation:

For an aspect ratio of 16 by 9, the stored value at address **15h** is 79 (4Fh).
For an aspect ratio of 16 by 10, the stored value at address **15h** is 61 (3Dh).
For an aspect ratio of 4 by 3, the stored value at address **15h** is 34 (22h).
For an aspect ratio of 5 by 4, the stored value at address **15h** is 26 (1Ah).

3-2. Portrait Orientation:

For an aspect ratio of 9 by 16, the stored value at address **16h** is 79 (4Fh).
For an aspect ratio of 10 by 16, the stored value at address **16h** is 61 (3Dh).
For an aspect ratio of 3 by 4, the stored value at address **16h** is 34 (22h).
For an aspect ratio of 4 by 5, the stored value at address **16h** is 26 (1Ah).

3.6.3 Display Transfer Characteristics (GAMMA): 1 Byte

The display transfer characteristic, referred to as GAMMA, is a required ELEMENT in EDID data structure version 1, revision 4. It shall be stored in a 1-byte field capable of representing GAMMA values in the range of 1.00 to 3.54. The integer value stored shall be determined by the formula:

Stored Value = (GAMMA x 100) – 100

Table 3.13 – Display Transfer Characteristics (GAMMA)

Address	1 Byte	Value	Description
17h	1	01h → FEh	Display Transfer Characteristic (GAMMA) (Range is from 1.00 → 3.54)
		FFh	If byte **17h** = FFh, then the GAMMA value is not defined here and the GAMMA data shall be stored in an extension block (e.g., DI-EXT).

Notes for Table 3.13:

1. The stored GAMMA is the factory default value as defined by the display manufacturer.
2. Example: For a GAMMA value of 2.2, the stored value at address **17h** is 120 (‘78h’).

3.6.4 Feature Support: 1 Byte

The feature support byte is a required ELEMENT in EDID structure version 1, revision 4. The feature support field shall be used to indicate support for various display features. The format of this 1-byte field is shown in Table 3.14.

Table 3.14 - Feature Support

Address	Bits Definitions			Description
18h	**7 6 5**	_ _	_ _ _	**Display Power Management:** (See Note 1) Bits 7 → 5
	1 _ _	_ _	_ _ _	Standby Mode is supported. Bit 7
	0 _ _	_ _	_ _ _	Standby Mode is not supported. Bit 7
	_ 1 _	_ _	_ _ _	Suspend Mode is supported. Bit 6
	_ 0 _	_ _	_ _ _	Suspend Mode is not supported. Bit 6
	_ _ 1	_ _	_ _ _	Active Off = Very Low Power is supported. Bit 5
	_ _ 0	_ _	_ _ _	Active Off = Very Low Power is not supported. Bit 5
		4 3	_ _ _	If bit 7 at address **14h** = '0' then bits 4 & 3 at address **18h** defines the **Display Color Type:** (See Note 2) Bits 4 & 3
		0 0	_ _ _	Monochrome or Grayscale display
		0 1	_ _ _	RGB color display
		1 0	_ _ _	Non-RGB color display
		1 1	_ _ _	Display Color Type is Undefined
		4 3	_ _ _	If bit 7 at address **14h** = '1' then bits 4 & 3 at address **18h** defines the **Supported Color Encoding Format/s:** (See Note 2) Bits 4 & 3
		0 0	_ _ _	RGB 4:4:4
		0 1	_ _ _	RGB 4:4:4 & YCrCb 4:4:4
		1 0	_ _ _	RGB 4:4:4 & YCrCb 4:2:2
		1 1	_ _ _	RGB 4:4:4 & YCrCb 4:4:4 & YCrCb 4:2:2
			2 1 0	**Other Feature Support Flags:** Bits 2 → 0
			1 _ _	sRGB Standard is the default color space. (See Note 3) Bit 2
			0 _ _	sRGB Standard is not the default color space. Bit 2
			_ 1 _	Preferred Timing Mode includes the native pixel format and preferred refresh rate of the display device. (See Note 4) Bit 1
			_ 0 _	Preferred Timing Mode does not include the native pixel format and preferred refresh rate of the display device. Bit 1
			_ _ 1	Display is continuous frequency. (See Note 5) Bit 0
			_ _ 0	Display is non-continuous frequency (multi-mode). Bit 0

Notes to Table 3.14:

1. DPM vs. DPMS: Note that VESA no longer supports the Display Power Management Signaling (DPMS) Standard. DPMS has been replaced by the Display Power Management (DPM) Standard. DPM defines two power modes: On and OFF. DPMS defines four power states: On, Standby, Suspend and Off. For legacy support, the following table defines the relationships (mappings) between the DPM and DPMS states.

Table 3.15 – DPMS vs. DPM --- State Mappings

DPMS State	DPM State	Industry Definition
ON	ON	ON
Standby	OFF	Sleep
Suspend	OFF	Sleep
Active OFF	OFF	Off, deep sleep or standby power

For DPM compliant displays, bit 5 at address 18h shall be set to 1 and bits 7 & 6 shall be set to 0. For DPMS compliant displays, bits 7, 6 and/or 5 shall be set to 1 indicating the supported power down modes.

2. Display Color Type vs. Supported Color Encoding Format(s): Refer to Table 3.11 for the definition of bit 7 at address **14h**.

3. Standard Default Color Space - sRGB: If this bit is set to 1, the display uses the sRGB standard default color space as its primary color space. If a display is sRGB compliant, then the color information in section 3.7 shall match the sRGB standard values.
4. Preferred Timing Mode: The display's preferred timing mode shall be listed in the first 18 byte data block (starting at address **36h**. Refer to section 3.10). This is a requirement for EDID data structure version 1, revision 3 and newer. For EDID version 1, revision 3, bit 1 (at address **18h)** shall be set to 1 (0 is invalid). For EDID version 1, revision 4, setting bit 1 (at address **18h)** to 1 indicates that the preferred timing mode includes the native pixel format and the preferred refresh rate of the display device (for example, an LCD module). A 0 at bit 1 (address **18h**) indicates the native pixel format and preferred refresh rate of the display device are not included in the preferred timing mode.
5. Continuous Frequency vs. Non-Continuous Frequency: For EDID version 1, revision 3, bit 0 (at address **18h**) indicated support for or no support for GTF (using the default GTF parameter values). For EDID version 1, revision 4, bit 0 (at address **18h**) has been redefined to indicate Continuous Frequency Display (set bit 0 to 1) or Non-Continuous Frequency (Multi-Mode) Display (set bit 0 to 0). If bit 0 is set to 1, then the display will accept GTF or CVT generated timings (from a source) that are within the display's range limits. Note that the displayed image may not be properly sized or centered. Use of the continuous frequency flag (bit 0 at address **18h**) is only required if the display manufacturer wants to enable the display to be used in a continuous frequency mode (as opposed to discrete timings specified elsewhere). If the continuous frequency bit is set to '1', then the Display Range Limits Descriptor (refer to section 3.10.3.3) is required to be included in BASE EDID. If bit 0 is set to 0, then the display is non-continuous frequency (multi-mode) and is only specified to accept the video timing formats that are listed in BASE EDID and certain EXTENSION Blocks. If the display supports GTF Secondary Curve refer to Table 3.27 in section 3.10.3.3.1. If the display is compliant with the CVT Standard, refer to table 3.28 in section 3.10.3.3.2.

3.7 Display x, y Chromaticity Coordinates: 10 Bytes

The display x, y chromaticity coordinates are required ELEMENTS in EDID data structure version 1, revision 4. These bytes provide chromaticity and white point information. The white point value shall be the default white point (the white point set at initial power on or after resetting the display to its default settings). The default white point is defined by the display manufacturer. The data shall be stored (as 10 bit numbers) in the order shown in Table 3.16. Provision for multiple white points can be made in one of the display descriptors - see Section 3.10.3.

Table 3.16 - Chromaticity and Default White Point

Address	10 Bytes	Color Characteristic	Byte Definitions
19h	1	Red / Green – bits 1 & 0	Rx1 Rx0 Ry1 Ry0 Gx1 Gx0 Gy1 Gy0
1Ah	1	Blue / White – bits 1 & 0	Bx1 Bx0 By1 By0 Wx1 Wx0 Wy1 Wy0
1Bh	1	Red_x	Red_x bits 9 → 2
1Ch	1	Red_y	Red_y bits 9 → 2
1Dh	1	Green_x	Green_x bits 9 → 2
1Eh	1	Green_y	Green_y bits 9 → 2
1Fh	1	Blue_x	Blue_x bits 9 → 2
20h	1	Blue_y	Blue_y bits 9 → 2
21h	1	White_x	White_x bits 9 → 2
22h	1	White_y	White_y bits 9 → 2

Notes to Table 3.16:

1. Stored data in Table 3.16 is based on the CIE 1931 (2°) Chromaticity Chart. Definitions of the CIE Chromaticity Chart can be found in CIE publication 15.2 (Colorimetry Space).

2. The chromaticity and white point values shall be expressed as fractional numbers, accurate to the thousandth place.
3. Each number shall be represented by a binary fraction, which is 10 bits in length. In this fraction a value of 1 for the bit immediately right of the decimal point (bit 9) represents 2 raised to the -1 power. A value of 1 in the right most bit (bit 0) represents a value of 2 raised to the -10 power.
4. The high order bits (9 → 2) shall be stored as a single byte. The low order bits (1 → 0) are paired with other low order bits to form a byte. With this representation, all values should be accurate to +/- 0.0005 of the specified value.
5. Monochrome displays shall indicate the appropriate white point x, y coordinates regardless of the actual color and shall set the red, green and blue x, y coordinates to '00h'.
6. Examples are shown in Table 3.17.

Table 3.17 - Ten bit Binary Fraction Representation

Actual Value	Binary value	Converted Back to Decimal
0.610	1001110001	0.6103516
0.307	0100111010	0.3066406
0.150	0010011010	0.1503906

3.8 Established Timings I & II: 3 bytes

The indication of support for established timings is optional in EDID data structure version 1, revision 4, except for displays that are VESA Plug & Play compliant. Plug & Play compliant displays shall show support for the BASE VIDEO MODE (640 × 480 @ 60Hz) and shall indicate support in the Established Timing I data field. The established timing data field is a list of one-bit flags, which may be used to indicate support for established VESA and other common timings in a very compact form. Other standardized timings may be described by the Standard Timings data field defined in Section 3.9. Any timing can be described using the Detailed Timings data field defined in Section 3.10.

Bits 6 → 0 (inclusive) of the byte at address **25h** may be used to define manufacturer's proprietary timings. These bits may be used if a manufacturer wants to identify such timings through the use of one-bit flags. VESA takes no responsibility for coordinating or documenting the use of these bits by any manufacturer(s).

In Table 3.18, a bit set to "1" shall indicate support for that timing.

Established Timings I & II indicate Factory Supported Modes of VESA DMT as well as other industry de-facto timings that predate EDID. The one-bit flags (either set or not set) of the Established Timing data field shall not be used to determine maximum format supported, maximum refresh supported, or any other timing parameter of the display. Any one-bit flag set to 1 in the Established Timing section shall indicate that this timing mode is a Factory Supported Mode. It shall not be used to determine the range limits of the display.

Factory Supported Modes **are defined as video timing modes which result in displayed images that are properly sized and centered (on the display's screen) as the display is delivered from factory.**

EDID may not indicate all Factory Supported Modes. Table 3.18 defines the Established Timings I & II.

Table 3.18 - Established Timings I & II

Address	3 Bytes	Bit #	Description	Source
23h	**1**		**Established Timing I**	
		7	720 x 400 @ 70Hz	IBM, VGA
		6	720 x 400 @ 88Hz	IBM, XGA2
		5	640 x 480 @ 60Hz	IBM, VGA
		4	640 x 480 @ 67Hz	Apple, Mac II
		3	640 x 480 @ 72Hz	VESA
		2	640 x 480 @ 75Hz	VESA
		1	800 x 600 @ 56Hz	VESA
		0	800 x 600 @ 60Hz	VESA
24h	**1**		**Established Timing II**	
		7	800 x 600 @ 72Hz	VESA
		6	800 x 600 @ 75Hz	VESA
		5	832 x 624 @ 75Hz	Apple, Mac II
		4	1024 x 768 @ 87Hz(I)	IBM - Interlaced
		3	1024 x 768 @ 60Hz	VESA
		2	1024 x 768 @ 70Hz	VESA
		1	1024 x 768 @ 75Hz	VESA
		0	1280 x 1024 @ 75Hz	VESA
25h	**1**		**Manufacturer's Timings**	
		7	1152 x 870 @ 75Hz	Apple, Mac II
		6-0	Reserved for Manufacturer Specified Timings	

3.9 Standard Timings: 16 Bytes

The use of standard timings is optional in EDID data structure version 1, revision 4. These 16 bytes provide identification for up to eight additional timings, each identified by a unique 2-byte code derived from the horizontal active pixel count, the image aspect ratio and field refresh rate as described in Table 3.19. The standard timing 2 byte codes for most VESA DMT definitions are listed in the latest revision of the DMT document. This scheme may also be used in display products intended to be used exclusively with proprietary systems where the host already has the complete timing information. Additional standard timings (2 byte codes) may be listed by using one of the alternate definitions of the Display Descriptors permitted in EDID Structure Version 1, Revision 1 and higher - see Section 3.10.3.

- Unused Standard Timing data fields shall be set to 01h, 01h.
- All Standard Timing identifiers are defined to be “Square Pixel” (1 : 1 pixel aspect ratio).

The Standard Timing data fields shall be used to identify Factory Supported Modes that fall into one or both of two categories:

- VESA Display Monitor Timings that are listed in the VESA and Industry Standards and Guidelines for Computer Display Monitor Timing (DMT) document.
- Display Monitor Timings not included in the DMT document and calculated using the CVT or GTF formula. Refer to Appendix B for an explanation of the relationship between standard timings, Generalized Timing Formula (GTF) and Coordinated Video Timing (CVT).

A 2-byte timing code identifies each Display Monitor Timing definition. If a timing code listed in EDID corresponds to an issued VESA Display Monitor Timing, factory adjustment data shall be stored (preset) in the display.

EDID may not indicate all Factory Supported Modes. Standard Timings definitions are shown in Table 3.19.

Table 3.19 - Standard Timings

Address	16 Bytes	Value		Description
	2			**Standard Timing 1:**
26h	**1**	01h → FFh		Value Stored (in hex) = (Horizontal addressable pixels ÷ 8) – 31 Range: 256 pixels → 2288 pixels, in increments of 8 pixels
		00h		Reserved: Do not use.
27h	**1**	**Bit Definitions**		**Description**
		7 6	_ _ _ _ _ _	**Image Aspect Ratio**: bits 7 & 6
		0 0	_ _ _ _ _ _	16 : 10 AR
		0 1	_ _ _ _ _ _	4 : 3 AR
		1 0	_ _ _ _ _ _	5 : 4 AR
		1 1	_ _ _ _ _ _	16 : 9 AR
			5 4 3 2 1 0	**Field Refresh Rate:** bits 5 → 0
			n n n n n n	Value Stored (in binary) = Field Refresh Rate (in Hz) – 60 Range: 60 Hz → 123Hz
28h, 29h	**2**	**Standard Timing 2:** Stored values use the Standard Timing 1 byte and bit definitions.		
2Ah, 2Bh	**2**	**Standard Timing 3:** Stored values use the Standard Timing 1 byte and bit definitions.		
2Ch, 2Dh	**2**	**Standard Timing 4:** Stored values use the Standard Timing 1 byte and bit definitions.		
2Eh, 2Fh	**2**	**Standard Timing 5:** Stored values use the Standard Timing 1 byte and bit definitions.		
30h, 31h	**2**	**Standard Timing 6:** Stored values use the Standard Timing 1 byte and bit definitions.		
32h, 33h	**2**	**Standard Timing 7:** Stored values use the Standard Timing 1 byte and bit definitions.		
34h, 35h	**2**	**Standard Timing 8:** Stored values use the Standard Timing 1 byte and bit definitions.		

Notes for Table 3.19:

1. The vertical addressable line count may be calculated from the aspect ratio and the horizontal addressable pixel count given in the first byte.
2. EDID structures prior to version 1, revision 3 defined the bit (bits 7 & 6 at address **27h**) combination of 0 0 to indicate a 1 : 1 aspect ratio.
3. Standard Timings shall not be used to define video timing modes with horizontal addressable pixel counts greater than 2288 pixels. In this case, the video timing mode shall be defined using the Detailed Timing Definition (Section 3.10.2) or the CVT Definition (Section 3.10.3.8).
4. Standard Timings shall not be used to define video timing modes with vertical field refresh rates greater than 123 Hz. In this case, the video timing mode shall be defined using the Detailed Timing Definition (refer to Section 3.10.2) or the CVT Definition (Section 3.10.3.8).

3.10 18 Byte Descriptors - 72 Bytes

NOTE: Previous versions of the VESA E-EDID Standard refer to the 18 Byte Descriptors as the Detailed Timing Blocks.

The 72 bytes in this section are divided into four data fields. Each of the four data fields are 18 bytes in length. These 18 byte data fields shall contain either detailed timing data as described in Section 3.10.2 or other types of data as described in Section 3.10.3. The addresses and the contents of the four 18 byte descriptors are shown in Table 3.20.

Table 3.20 - 18 Byte Descriptors

Addresses	Field Name	Description
36h → 47h	First 18 Byte Descriptor	Preferred Timing Mode is a requirement.
48h → 59h	Second 18 Byte Descriptor	2nd Detailed Timing Descriptor or the 1st Display Descriptor
5Ah → 6Bh	Third 18 Byte Descriptor	3rd Detailed Timing Descriptor or the 2nd Display Descriptor
6Ch → 7Dh	Fourth 18 Byte Descriptor	4th Detailed Timing Descriptor or the 3rd Display Descriptor

Notes for Table 3.20:
Use of these 18 Byte Data Descriptors shall meet the following requirements:

1. Each of the four data blocks shall contain a detailed timing descriptor, a display descriptor or a dummy descriptor (Tag 10h) using definitions described in Sections 3.10.2 and 3.10.3. Use of a data fill pattern is not permitted - the Dummy Descriptor (Tag 10h) is the only exception.
2. Detailed timing mode descriptors shall represent a supported video timing mode of the display.
3. The 18 byte descriptors shall be ordered such that all detailed video timing descriptors precede other types of display descriptor fields.
4. The first 18 byte descriptor field shall be used to indicate the display's preferred timing mode. This is described in Section 3.10.1. The display's preferred timing mode is a required ELEMENT in EDID data structure version 1, revision 4.
5. A Display Range Limits Descriptor (which was required in EDID data structure version 1, revision 3) is optional (but recommended) in EDID data structure version 1, revision 4. Continuous frequency displays (which may support GTF or CVT) are required to include the Display Range Limit Descriptor.
6. A Display Product Name Descriptor (required in EDID data structure version 1, revision 3) is optional (but recommended) in EDID data structure version 1, revision 4.
   Examples:
   Example A: Preferred Detailed Timing, Detailed Timing 2, Monitor Range Limits, Monitor Name.
   Example B: Preferred Detailed Timing, Monitor Range Limits, Monitor Name, Monitor Serial Number.
   Example C: Preferred Detailed Timing, Detailed Timing 2, Detailed Timing 3, Detailed Timing 4.

Note on EDID Data Structure Version 1, Revision 3: Items 4, 5 and 6 above were permitted but not required prior to EDID data structure version 1 revision 3. Hosts may encounter displays using EDID version 1 revision 0→2 which do not meet all of these requirements.
Note on EDID Data Structure Version 1, Revision 4: Item 4 is still required in EDID data structure version 1, revision 4. Items 5 and 6 above are optional but recommended. Certain markets require the display range limits and the display product name descriptors in order to be compliant with certain operating system logo certification programs.

3.10.1 The First 18 Byte Descriptor

The first 18 Byte Descriptor Block shall contain the preferred timing mode. The display manufacturer defines the “Preferred Timing Mode (PTM)” as the video timing mode that will produce the best quality image on the display’s viewing screen. The display manufacturer defines the meaning of the words “best quality image”. For most flat panel displays (FPD), the preferred timing mode will be the panel’s "native timing" based on its “native pixel format”.

3.10.2 Detailed Timing Descriptor: 18 bytes

The 18 byte detailed timing descriptor (stored in the 18 Byte Descriptors) is defined in Tables 3.21 & 3.22. Detailed timing descriptors may be defined in one, two, three or all four of the 18 byte descriptor fields. Refer to Section 3.10 for restrictions.

Table 3.21 - Detailed Timing Definition --- Part 1

Byte #	# of Bytes	Value	Detailed Timing Definitions
0, 1	2	(00 01)h → (FF FF)h	Stored Value = Pixel clock ÷ 10,000 LSB stored in byte 0 and MSB stored in byte 1 Range: 10 kHz to 655.35 MHz in 10 kHz steps
		(00 00)h	Reserved: Do not use for Detailed Timing Descriptor
2	1	00h → FFh	Horizontal Addressable Video in pixels --- contains lower 8 bits
3	1	00h → FFh	Horizontal Blanking in pixels --- contains lower 8 bits
4	1	({HA}h, {HB}h) where 0h ≤ HA ≤ Fh and 0h ≤ HB ≤ Fh	Horizontal Addressable Video in pixels – -- stored in Upper Nibble : contains upper 4 bits
			Horizontal Blanking in pixels --- stored in Lower Nibble : contains upper 4 bits
5	1	00h → FFh	Vertical Addressable Video in lines --- contains lower 8 bits
6	1	00h → FFh	Vertical Blanking in lines --- contains lower 8 bits
7	1	({VA}h, {VB}h) where 0h ≤ VA ≤ Fh and 0h ≤ VB ≤ Fh	Vertical Addressable Video in lines -- stored in Upper Nibble : contains upper 4 bits
			Vertical Blanking in lines --- stored in Lower Nibble : contains upper 4 bits
8	1	00h → FFh	Horizontal Front Porch in pixels --- contains lower 8 bits
9	1	00h → FFh	Horizontal Sync Pulse Width in pixels --- contains lower 8 bits
10	1	({VF}h, {VS}h) where 0h ≤ VF ≤ Fh and 0h ≤ VS ≤ Fh	Vertical Front Porch in Lines --- stored in Upper Nibble : contains lower 4 bits
			Vertical Sync Pulse Width in Lines --- stored in Lower Nibble : contains lower 4 bits
		7 6 5 4 3 2 1 0	**Bit Definitions**
11	1	n n _ _ _ _ _ _	Horizontal Front Porch in pixels --- contains upper 2 bits
		_ _ n n _ _ _ _	Horizontal Sync Pulse Width in Pixels --- contains upper 2 bits
		_ _ _ _ n n _ _	Vertical Front Porch in lines --- contains upper 2 bits
		_ _ _ _ _ _ n n	Vertical Sync Pulse Width in lines --- contains upper 2 bits
		Value	**Video Image Size & Border Definitions**
12	1	00h → FFh	Horizontal Addressable Video Image Size in mm --- contains lower 8 bits
13	1	00h → FFh	Vertical Addressable Video Image Size in mm --- contains lower 8 bits
14	1	({HI}h, {VI}h) where 0h ≤ HI ≤ Fh and 0h ≤ VI ≤ Fh	Horizontal Addressable Video Image Size in mm --- stored in Upper Nibble : contains upper 4 bits
			Vertical Addressable Video Image Size in mm --- stored in Lower Nibble : contains upper 4 bits
15	1	00h → FFh	Right Horizontal Border or Left Horizontal Border in pixels --- refer to Section 3.12 – Right Border is equal to Left Border
16	1	00h → FFh	Top Vertical Border or Bottom Vertical Border in Lines --- refer to Section 3.12 – Top Border is equal to Bottom Border

Notes for Table 3.21:

1. Pixel Clock Example: A Pixel Clock of 135MHz would be represented by 13500 decimal which is stored as BCh, 34h.
2. Horizontal Addressable Video is represented by a 12 bit number (Upper nibble of byte 4 and the 8 bits of byte 2) - Range is 0 pixels to 4095 pixels.
3. Horizontal Blanking is represented by a 12 bit number (Lower nibble of byte 4 and the 8 bits of byte 3) - Range is 0 pixels to 4095 pixels.

4. Vertical Addressable Video is represented by a 12 bit number (Upper nibble of byte 7 and the 8 bits of byte 5) - Range is 0 lines to 4095 lines.
5. Vertical Blanking is represented by a 12 bit number (Lower nibble of byte 7 and the 8 bits of byte 6) - Range is 0 lines to 4095 lines.
6. **Note:** Previous versions of the E-EDID Standard refer to the "H or V Front Porch" as the "H or V Sync Offset".
7. Horizontal Front Porch in Pixels (from blanking start to start of sync) is represented by a 10 bit number (Bits 7 & 6 of byte 11 and the 8 bits of byte 8) - Range is 0 pixels to 1023 pixels.
8. Horizontal Sync Pulse Width in Pixels (from the end of the front porch to the start of the back porch) is represented by a 10 bit number (Bits 5 & 4 of byte 11 and the 8 bits of byte 9) - Range is 0 pixels to 1023 pixels.
9. Vertical Front Porch in Lines (from blanking start to start of sync) is represented by a 6 bit number (Bits 3 & 2 of byte 11 and the upper nibble of byte 10) - Range is 0 lines to 63 lines.
10. Vertical Sync Pulse Width in Lines (from the end of the front porch to the start of the back porch) is represented by a 6 bit number (Bits 1 & 0 of byte 11 and the lower nibble of byte 10 - Range is 0 lines to 63 lines.
11. Horizontal Addressable Video Image Size in mm is represented by a 12 bit number (Upper nibble of byte 14 and the 8 bits of byte 12) - Range is 0 mm to 4095 mm.
12. Vertical Addressable Video Image Size in mm is represented by a 12 bit number (Lower nibble of byte 14 and the 8 bits of byte 13) - Range is 0 mm to 4095 mm.
13. Right Horizontal Border or Left Horizontal Border in Pixels is represented by an 8 bit number (the 8 bits of byte 15) - Range is 0 pixels to 255 pixels.
14. Top Vertical Border or Bottom Vertical Border in Lines is represented by an 8 bit number (the 8 bits of byte 16) - Range is 0 lines to 255 lines.
15. Horizontal and vertical screen size fields in Table 3.12 define the active physical screen size of the display device. The active physical screen size is defined as the rectangular area where light can be controlled on the display. The horizontal and vertical addressable video image size fields in Table 3.21 define the addressable video size of the displayed image (derived from the incoming video signal).
    For Example: When a 16 : 9 AR video signal with 1280 x 720 pixels is displayed on a 5 : 4 AR screen with 1280 x 1024 pixels, the horizontal image size in table 3.21 will be equal to the horizontal screen size in table 3.12. And the vertical image size in Table 3.21 will be less than the vertical screen size listed in table 3.12 (common term is "letterbox").
    Another Example: When a 5 : 4 AR video signal with 1280 x 1024 pixels is displayed on a 16 : 9 AR screen with 1920 x 1080 pixels, the vertical image size in Table 3.21 will be equal to the vertical screen size in Table 3.12. And the horizontal image size in table 3.21 will be less than the horizontal screen size listed in Table 3.12 (common term is "pillarbox"). These examples assume that the scaling function (in the display) maintains the image aspect ratio of the video content while scaling the image up (or down) to the maximum horizontal or vertical screen size listed in Table 3.12.
16. The horizontal and vertical addressable video image sizes in Table 3.21 shall be less than or equal to the maximum horizontal and vertical screen sizes listed in Table 3.12.
17. For certain types of display products (for example front projectors with image zoom controls), the horizontal and vertical addressable video image sizes in Table 3.21 and screen sizes in table 3.12 are undefined and these fields shall be set to 0 mm and 0 cm, respectively.
18. Image Size vs. Aspect Ratio:
    18.1 For Information Technology (IT) timing modes, the source can determine the aspect ratio of the displayed image by looking at the number of horizontal pixels and the number of vertical lines listed in the detailed timing descriptor. Display manufacturers shall include the displayed image size (in mm) in the detailed timing descriptor. **Exception** – refer to note 17.

18.2 For Digital Television (DTV) timing modes, the display manufacturer has the option to define the aspect ratio of the DTV timing mode by listing 16 mm by 9 mm or 4 mm by 3 mm in the Image Size data field (bytes 12, 13 & 14).

19. Refer to Section 3.12 for the definitions of the video timing parameters listed in Table 3.21.

Table 3.22 - Detailed Timing Definition --- Part 2

Byte #	# of Bytes	Bit Definitions								Detailed Timing Definitions
		7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Signal Interface Type:**
		0	_	_	_	_	_	_	_	Non-Interlaced (1 frame = 1 field)
		1	_	_	_	_	_	_	_	Interlaced (1 frame = 2 fields)
		_	**6**	**5**	_	_	_	_	**0**	**Stereo Viewing Support:**
			0	0	_	_	_	_	x	Normal Display – No Stereo. The value of bit 0 is "don't care"
			0	1	_	_	_	_	0	Field sequential stereo, right image when stereo sync signal = 1
			1	0	_	_	_	_	0	Field sequential stereo, left image when stereo sync signal = 1
			0	1	_	_	_	_	1	2-way interleaved stereo, right image on even lines
			1	0	_	_	_	_	1	2-way interleaved stereo, left image on even lines
			1	1	_	_	_	_	0	4-way interleaved stereo
			1	1	_	_	_	_	1	Side-by-Side interleaved stereo
		_	_	_	**4**	**3**	**2**	**1**	_	**Analog Sync Signal Definitions:**
					0	0	_	_	_	Analog Composite Sync:
17	1				0	1	_	_	_	Bipolar Analog Composite Sync:
					0	_	0	_	_	---------- Without Serrations;
					0	_	1	_	_	---------- With Serrations (H-sync during V-sync);
					0	_	_	0	_	---------- Sync On Green Signal only
					0	_	_	1	_	---------- Sync On all three (RGB) video signals
		_	_	_	**4**	**3**	**2**	**1**	_	**Digital Sync Signal Definitions:**
					1	0	_	_	_	Digital Composite Sync:
					1	0	0	_	_	---------- Without Serrations;
					1	0	1	_	_	---------- With Serrations (H-sync during V-sync);
					1	1	_	_	_	Digital Separate Sync:
					1	1	0	_	_	---------- Vertical Sync is Negative;
					1	1	1	_	_	---------- Vertical Sync is Positive;
					1	_	_	0	_	---------- Horizontal Sync is Negative (outside of V-sync)
					1	_	_	1	_	---------- Horizontal Sync is Positive (outside of V-sync)

Notes for Table 3.22: The following includes definitions for the labels in bits 4 & 3 of Table 3.22:

1. Analog Composite: Analog video standards embed the sync in the video signal, in the luminance channel (for Y/C, or in the case of composite video it still winds up basically in the same place), or in PC standards typically in the green channel of RGB analog video. Composite sync refers to any situation in which horizontal and vertical sync signals are carried in the same physical channel. Whether or not the vertical sync signal is "serrated" (i.e., contains horizontal sync pulses of the opposite polarity than normal) is a separate question. Typically in analog video signals, sync is carried as a "blacker than black" negative-going pulse (i.e., in the RS-343A standard, using the blanking level as the reference point, the sync tips are nominally -0.286V from blank, while the reference white level is +0.714V, for an overall 1.000 Vp-p signal).
2. Bipolar Analog Composite: For digital television, there are standards for analog component video interfaces defining timings for standard definition (SD), enhanced definition (ED) and high definition (HD) signals. A bipolar sync is defined for the SD and ED timings. A tri-level sync is defined for the HD timings. Both sync types are found only on the luminance (Y) signal; no sync pulses are present on either the 'Pb' or 'Pr' signals. The bipolar sync (in reference to the blanking level) is a negative pulse having an amplitude of -300 mV. The tri-level sync pulse will start at the zero volt level and transition to -300 mV. The next transition is +300 mV and then returns to

the zero volts level. The zero crossing is the sync reference. Although defined in the HD standards, the tri-level sync is generally not utilized by consumer equipment. The bipolar sync is typically used instead.

3. Digital Composite: Typically, "digital sync" refers to a situation in which the syncs are carried on a separate physical channel from the video signal (as in the "VGA" interface common in PCs, which has analog RGB video but discrete TTL sync lines). "Composite" here again refers to the case in which both horizontal and vertical syncs are combined into a single signal, most commonly carried on what would otherwise be the "horizontal" sync line.
4. Digital Separate: The horizontal and vertical syncs are carried separately (on "digital" lines) from the analog video signals, but in this case the horizontal and vertical syncs are also kept physically separate. This is the most common form of sync used in analog PC video interfaces such as the VGA interface.
5. **Note** that neither (3) or (4) above refers to a "fully-digital" display interface; in these cases, the horizontal and vertical sync information is generally embedded within the same data stream that carries the video information, and so cannot be physically isolated within the interface itself. The syncs will commonly be provided in separate form by the receiver device.

3.10.3 Display Descriptor Definitions - 18 bytes

The use of display descriptors is optional in EDID structure version 1, revision 4. The first 18 byte descriptor (at addresses **36h → 47h)** shall contain the Preferred Timing Mode (refer to Section 3.10.1). The remaining three 18-byte descriptors (at addresses **48h → 59h**, **5Ah → 6Bh** and **6Ch → 7Dh**) may contain video timing definitions (refer to section 3.10.2) or alternately be defined as optional Display Descriptors using the general format shown in Table 3.23. Detailed descriptions of the data types are shown in Tables 3.24 → 3.36. Those 18-byte descriptors not used for Display Descriptors shall be used for detailed timings.

Table 3.23 - Display Descriptor Summary

Byte #	# of Bytes	Values	Display Descriptor Definitions
0, 1	2	(00 00)h	Indicates that this 18 byte descriptor is a Display Descriptor.
2	1	00h	Reserved: Set to 00h when 18 byte descriptor is used as a Display Descriptor
		Tag	**Display Descriptor Tag Numbers**
3	1	FFh	Display Product Serial Number: Defined in Section 3.10.3.1
		FEh	Alphanumeric Data String (ASCII): Defined in Section 3.10.3.2
		FDh	Display Range Limits: Includes optional timing information --- GTF using default parameters, GTF Secondary Curve or CVT Descriptor. Defined in Section 3.10.3.3
		FCh	Display Product Name: Defined in Section 3.10.3.4
		FBh	Color Point Data: Defined in Section 3.10.3.5
		FAh	Standard Timing Identifications: Defined in Section 3.10.3.6
		F9h	Display Color Management (DCM) Data: Defined in Section 3.10.3.7
		F8h	CVT 3 Byte Timing Codes: Defined in Section 3.10.3.8
		F7h	Established Timings III Defined in Section 3.10.3.9
		11h → F6h	Reserved: Currently undefined -- Do Not Use Refer to Section 3.10.3.10
		10h	Dummy Descriptor: Defined in Section 3.10.3.11
		00h → 0Fh	Manufacturer Specified Display Descriptors: Defined in Section 3.10.3.12
4	1	00h	Reserved: Set to 00h when 18 byte descriptor is used as a Display Descriptor Exception: Refer to Display Range Limits Descriptor (Tag FDh) – Section 3.10.3.3
5 → 17	13	00h → FFh	Stored data dependant on Display Descriptor Definition

Notes for Table 3.23:

1. The first three bytes of the block shall be '000000h', when the 18 byte descriptor contains a display descriptor (not a detailed timing). The fourth byte shall contain the display descriptor tag number (from Table 3.23) and the fifth byte shall be '00h'.
2. It should be noted here that VESA has decided to replace the GTF Standard with the CVT Standard. The GTF Standard will be (or is) deprecated. For the purpose of GTF legacy support, EDID data structure version 1, revision 4 still supports GTF. However, VESA recommends that all new designs (where appropriate) use CVT.

3.10.3.1 Display Product Serial Number Descriptor Definition (tag #FFh)

Up to 13 characters (using ASCII codes) of a serial number may be stored in the Display Product Serial Number Descriptor (tag #FFh). The data shall be sequenced such that the 1st byte (ASCII code) = the 1st character, the 2nd byte (ASCII code) = the 2nd character, etc. If there are less than 13 characters in the string, then terminate the serial number string with ASCII code '0Ah' (line feed) and pad the unused bytes in the field with ASCII code '20h' (space). Table 3.24 defines the format. Refer to Appendix E for ASCII Reference Tables.

Table 3.24 – Display Product Serial Number Descriptor Definition

Byte #	Value	Display Product Serial Number Definition
0, 1	(00 00)h	Indicates that this 18 byte descriptor is a Display Descriptor.
2	00h	Reserved: Set to 00h when 18 byte descriptor is used as a Display Descriptor
3	FFh	Display Product Serial Number Descriptor Tag Number:
4	00h	Reserved:
5 → 17	00h → FFh	Up to 13 alphanumeric characters of a serial number may be stored.

For Example: S/N is 'A0123456789' is stored as '00h 00h 00h FFh 00h 41h 30h 31h 32h 33h 34h 35h 36h 37h 38h 39h 0Ah 20h'.

3.10.3.2 Alphanumeric Data String Descriptor Definition (tag #FEh)

Up to 13 characters (using ASCII codes) of a data string may be stored in the Alphanumeric Data String Descriptor (tag #FEh). The data shall be sequenced such that the 1st byte (ASCII code) = the 1st character, the 2nd byte (ASCII code) = the 2nd character, etc. If there are less than 13 characters in the string, then terminate the alphanumeric data string with ASCII code '0Ah' (line feed) and pad the unused bytes in the field with ASCII code '20h' (space). Table 3.25 defines the format. Refer to Appendix E for ASCII Reference Tables.

Table 3.25 – Alphanumeric Data String Descriptor Definition

Byte #	Value	Alphanumeric Data String Definition
0, 1	(00 00)h	Indicates that this 18 byte descriptor is a Display Descriptor.
2	00h	Reserved: Set to 00h when 18 byte descriptor is used as a Display Descriptor
3	FEh	Alphanumeric Data String Descriptor Tag Number:
4	00h	Reserved:
5	00h → FFh	Up to 13 alphanumeric characters of a data string may be stored.

Notes for Table 3.25:

1. For Example: ASCII Data String is 'THISISATEST' is stored as '00h 00h 00h FEh 00h 54h 48h 49h 53h 49h 53h 41h 54h 45h 53h 54h 0Ah 20h'".
2. Note: Refer to VESA's LS-EXT Standard for using localization (native language) strings in an extension block.

3.10.3.3 Display Range Limits & Additional Timing Descriptor Definition (tag #FDh)

The use of the Display Range Limit Descriptor is optional in EDID version 1, revision 4. The range limits (minimum & maximum) of the vertical scanning rate and the horizontal scanning rate as well as the maximum supported pixel clock frequency shall be declared in the Display Range Limits Descriptor (tag #FDh). Refer to Table 3.26. For EDID Structure Version 1, Revision 4, the use of the display range limits descriptor is optional (but recommended). Refer to Note 5 of Table 3.14.

The Display Range Limits Descriptor will include one of the following sets of information:
1. Range Limits Only --- no additional timing information provided (defined in table 3.26) - Default GTF, GTF Secondary Curve and CVT are not supported or
2. Range Limits provided & Default GTF is supported - no additional timing information provided (defined in Table 3.26) or
3. Range Limits provided & GTF Secondary Curve Timing Formula is supported – Secondary GTF Curve Data (defined in Table 3.27) or
4. Range Limits provided & CVT Timing Formula is supported – Coordinated Video Timing Data (defined in Table 3.28).

Table 3.26 – Display Range Limits & Timing Descriptor Block Definition

Byte #	Value	Display Range Limits Definitions
0, 1	(00 00)h	Indicates that this 18 byte descriptor is a Display Descriptor.
2	00h	Reserved: Set to 00h when 18 byte descriptor is used as a Display Descriptor
3	FDh	Tag Number for Display Range Limits Descriptor
4	**7 6 5 4 3 2 1 0**	**Display Range Limits Offsets:** FLAGs
	0 0 0 0 _ _ 0 0	Vertical Rate Offsets are zero.
	0 0 0 0 _ _ 1 0	Max. Vertical Rate + 255 Hz Offset; Min. Vertical Rate is not offset
	0 0 0 0 _ _ 1 1	Max. Vertical Rate + 255 Hz Offset; Min. Vertical Rate + 255 Hz Offset
	0 0 0 0 0 0 _ _	Horizontal Rate Offsets are zero.
	0 0 0 0 1 0 _ _	Max. Horizontal Rate + 255 kHz Offset; Min. Horizontal Rate is not offset
	0 0 0 0 1 1 _ _	Max. Horizontal Rate + 255 kHz Offset; Min. Horizontal Rate + 255 kHz Offset
	01h, 04h → 07h, 09h, 0Dh 10h → FFh	Reserved: Do not use.
5	01h → FFh	**Minimum Vertical Rate:** (for interlace this refers to the field rate)
	[Byte 4, Bits 1, 0] ≠ 11	Binary coded rate in Hz, integer only (range is 1 Hz to 255 Hz)
	[Byte 4, Bits 1, 0] = 11	Binary coded rate in Hz, integer only (range is 256 Hz to 510 Hz)
	00h	Reserved: Do Not Use.
6	01h → FFh	**Maximum Vertical Rate:** (for interlace this refers to the field rate)
	[Byte 4, Bit 1] ≠ 1	Binary coded rate in Hz, integer only (range is 1 Hz to 255 Hz)
	[Byte 4, Bit 1] = 1	Binary coded rate in Hz, integer only (range is 256 Hz to 510 Hz)
		Note: *Minimum rate value shall be less than or equal to maximum rate value*
	00h	Reserved: Do Not Use.
7	01h → FFh	**Minimum Horizontal Rate:**
	[Byte 4, Bits 3, 2] ≠ 11	Binary coded rate in kHz, integer only (range is 1 kHz to 255 kHz)
	[Byte 4, Bits 3, 2] = 11	Binary coded rate in kHz, integer only (range is 256 kHz to 510 kHz)
	00h	Reserved: Do Not Use.
8	01h → FFh	**Maximum Horizontal Rate:**
	[Byte 4, Bit 3] ≠ 1	Binary coded rate in kHz, integer only (range is 1 kHz to 255 kHz)
	[Byte 4, Bit 3] = 1	Binary coded rate in kHz, integer only (range is 256 kHz to 510 kHz)
		Note: *Minimum rate value shall be less than or equal to maximum rate value*
	00h	Reserved: Do Not Use.
9	01h → FFh	**Maximum Pixel Clock:**
		Binary coded clock rate in MHz ÷ 10, *Example: 130MHz is '0Dh'*
		Note: *Maximum Pixel Clock shall be rounded to the nearest multiple of 10 MHz.*
	00h	Reserved: Do Not Use.
10		**Video Timing Support Flags:** Bytes 10 → 17 indicate support for additional video timings.
	00h	Default GTF supported if bit 0 in Feature Support Byte at address **18**h = 1
	01h	Range Limits Only --- no additional timing information is provided.
	02h	Secondary GTF supported --- requires support for Default GTF
	04h	CVT supported if bit 0 in Feature Support Byte at address **18**h = 1
	03h, 05h → FFh	Reserved for future timing definitions --- Do Not Use.
11	0Ah	Line Feed (if Byte 10 = 00h or 01h)
	00h → FFh	Video Timing Data (if Byte 10 = 02h or 04h) --- Refer to Tables 3.27 → 3.28
12 → 17	20h	Space (if Byte 10 = 00h or 01h)
	00h → FFh	Video Timing Data (if Byte 10 = 02h or 04h) --- Refer to Tables 3.27 → 3.28

Notes for Table 3.26:

1. For EDID Structure Version 1, Revision 4, the use of the display range limits descriptor is optional (but recommended). However, the Display Range Limits shall be included in the BASE EDID, if bit 0 of the Feature Support Byte at address **18h** is set to 1 (indicating a continuous frequency display).
2. Any timing outside these limits may cause the display to enter a self-protection mode (out of range error) or may cause damage to the display. The host shall always verify that an intended timing falls within these limits before the timing is applied - assumes that the Display Range Limits are defined.
3. Video Timing Support Flag (in Byte 10) = 00h and bit 0 of the Feature Support Byte at address **18h** set to 1 (indicating a continuous frequency display) indicates that this display supports GTF generated video timing modes using the default GTF parameters. If Byte 10 = 00h, then bit 0 of the Feature Support Byte at address **18h** shall not be set to 0 (indicating a non-continuous frequency multi-mode display). All GTF compliant displays are continuous frequency.
4. Video Timing Support Flag (in Byte 10) = 01h and bit 0 of the Feature Support Byte at address **18h** set to 1 (indicating a continuous frequency display) indicates that this display will present an image with any valid video mode timing within the Display Range Limits defined by Bytes 5 → 9. The displayed image may not be properly sized or centered. If bit 0 of the Feature Support Byte at address **18h** set to 0 (indicating a non-continuous frequency multi-mode display) indicates that this display will only present an image with the valid video mode timings (declared in the Established, Standard and Detailed Timings) that are listed in the BASE EDID or any EXTENSION Block.
5. Video Timing Support Flag (in Byte 10) = 02h and bit 0 of the Feature Support Byte at address **18h** set to 1 (indicating a continuous frequency display) indicates that this display supports GTF generated video timing modes using the default GTF parameters and GTF Secondary Curve parameters (refer to Table 3.27). If Byte 10 = 02h, then bit 0 of the Feature Support Byte at address **18h** shall not be set to 0 (indicating a non-continuous frequency multi-mode display). All GTF compliant displays are continuous frequency.
6. Video Timing Support Flag (in Byte 10) = 04h and bit 0 of the Feature Support Byte at address **18h** set to 1 (indicating a continuous frequency display) indicates that this display supports Coordinated Video Timing (CVT) generated video timing modes using the CVT parameters defined in table 3.28. If Byte 10 = 04h, then bit 0 of the Feature Support Byte at address **18h** shall not be set to 0 (indicating a non-continuous frequency multi-mode display). All CVT compliant displays are continuous frequency.
7. All video timing modes (listed in BASE EDID or timing extensions) shall be supported by the display and the frequencies for the listed video timing modes shall fall within the minimum and maximum horizontal and vertical frequency range limits.
8. Use of the continuous frequency flag (bit 0 at address **18h**) is only required if the display manufacturer wants to enable the display to be used in a continuous frequency mode (as opposed to discrete timings specified elsewhere). If the continuous frequency bit is set to '1', then the Display Range Limits Descriptor (refer to Section 3.10.3.3) is required to be included in BASE EDID.
9. "Range Limits Only" (byte 10) indicates that the display supports only those video timing modes that are listed in BASE EDID or certain EXTENSION blocks.

3.10.3.3.1 Display Range Limits with GTF Secondary Curve Definition:

With EDID Structure version 1, revision 4, GTF has been ***Deprecated*** (GTF is considered obsolete and in the process of being phased out) in favor of CVT. GTF has been retained in EDID Structure version 1, revision 4 for legacy support only and may be retired in a future release of the E-EDID Standard. VESA no longer recommends using GTF. Table 3.27 defines support for the GTF

Secondary Timing Curve Formula. Refer to the VESA Generalized Timing Formula (GTF) Standard for more information on the timing parameters listed in Table 3.27.

Table 3.27 – Display Range Limits & GTF Secondary Curve Block Definition

Byte #	Value	GTF Secondary Curve Definitions
0 → 9	00h → FFh	**Defines Display Range Limits:** Refer to Table 3.26
10	02h	Indicates GTF Secondary Curve supported: (with Continuous Video Timings)
11	00h	Reserved: Shall be set to '00h'
12	00h → FFh	Start break frequency for secondary curve: ((Horizontal Frequency) ÷ 2) kHz
13	00h → FFh	C × 2: (range is 0 ≤ C ≤ 127)
14, 15	(00 00)h → (FF FF)h	M: (range is 0 ≤ M ≤ 65,535) --- Value of M stored as LSB first.
16	00h → FFh	K: (range is 0 ≤ K ≤ 255)
17	00h → FFh	J × 2: (range is 0 ≤ J ≤ 127)

Notes for Table 3.27:

1. A display that supports GTF (Secondary Curve) shall also support the GTF (Default) and bit 0 in the Feature Support Byte (at address **18h**) shall be set to '1'.
2. If a display supports GTF (Default only) or GTF (Default and Secondary Curve) the EDID table shall include the Display Range Limits (refer to Table 3.26).

3.10.3.3.2 Display Range Limits with CVT Support Definition:

For displays that support the VESA CVT Standard, you have the option to include CVT support information in the Display Range Limits Descriptor. Table 3.28 defines support for CVT. Refer to the VESA CVT Standard for more information on the timing parameters listed in Table 3.28.

Table 3.28 – Display Range Limits & CVT Support Definition

Byte #	Value	CVT Support Definitions
0 → 9	00h → FFh	**Defines Display Range Limits:** Refer to Table 3.26
10	04h	Indicates CVT supported: (with Continuous Video Timings)
11	1h → Fh; 0h → Fh	CVT Standard Version Number: e.g. '11h' implies "Version 1.1"
12	**7 6 5 4 3 2** _ _	**Additional Pixel Clock Precision:**
	0 0 0 0 0 0 _ _	6 bits of extra pixel clock resolution for 0.25 MHz accuracy
	to	Max. Pix Clk = [(Byte 9) × 10] – [(Byte 12: bits 7 → 2) × 0.25MHz]
	1 1 1 1 1 1 _ _	Byte 9 is rounded up to the nearest multiple of 10 MHz
	_ _ _ _ _ _ **1 0**	**Maximum Active Pixels per Line - Most Significant Bits:**
	_ _ _ _ _ _ n n	Range is 00 → 11
13	**7 6 5 4 3 2 1 0**	**Maximum Active Pixels per Line - Least Significant Bits:**
	0 0 0 0 0 0 0 0	Indicates that there is no limit on the number of Horiz. Active Pixels
	0 0 0 0 0 0 0 1	Maximum Active Pixels per Line - Least Significant Bits
	to	Maximum Horizontal Active Pixels =
	1 1 1 1 1 1 1 1	8 × [Byte 13 + (256 × (Byte 12: bits 1, 0))]
14	**7 6 5 4 3 2 1 0**	**Supported Aspect Ratios:**
	1 _ _ _ _ 0 0 0	4 : 3 AR
	_ 1 _ _ _ 0 0 0	16 : 9 AR
	_ _ 1 _ _ 0 0 0	16 : 10 AR
	_ _ _ 1 _ 0 0 0	5 : 4 AR
	_ _ _ _ 1 0 0 0	15 : 9 AR
	_ _ _ _ _ 0 0 0	Reserved Bits: Shall be set to '000'.
15	**7 6 5 2 1 0**	**Preferred Aspect Ratio:**
	0 0 0 _ _ 0 0 0	4 : 3 AR
	0 0 1 _ _ 0 0 0	16 : 9 AR
	0 1 0 _ _ 0 0 0	16 : 10 AR
	0 1 1 _ _ 0 0 0	5 : 4 AR
	1 0 0 _ _ 0 0 0	15 : 9 AR
	n n n _ _ 0 0 0	Reserved Values: 'nnn' = '101' → '111' shall not be used.
	4 3	**CVT Blanking Support:**
	_ _ _ _ 0 0 0 0	Standard CVT Blanking is not supported.
	_ _ _ _ 1 0 0 0	Standard CVT Blanking is supported.
	_ _ _ 0 _ 0 0 0	Reduced CVT Blanking is not supported.
	_ _ _ 1 _ 0 0 0	Reduced CVT Blanking is supported (preferred).
	_ _ _ _ _ 0 0 0	Reserved Bits: Shall be set to '000'.
16	**7 6 5 4 3 2 1 0**	**Type of Display Scaling Supported:**
	1 _ _ _ 0 0 0 0	Horizontal Shrink
	_ 1 _ _ 0 0 0 0	Horizontal Stretch
	_ _ 1 _ 0 0 0 0	Vertical Shrink
	_ _ _ 1 0 0 0 0	Vertical Stretch
	_ _ _ _ 0 0 0 0	Reserved Bits: Shall be set to '0000'.
17	01h → FFh	**Preferred Vertical Refresh Rate:** Rate is in Hz; Integer Value only.
	00h	Reserved Value: '00h' shall not be used.

Notes for Table 3.28:

1. Horizontal Shrink: Input horizontal active pixel count can be greater than the preferred horiz. pixel count.
2. Horizontal Stretch: Input horizontal active pixel count can be less than the preferred horiz. pixel count.
3. Vertical Shrink: Input vertical active line count can be greater than the preferred vert. line count.
4. Vertical Stretch: Input vertical active line count can be less than the preferred vert. line count.

3.10.3.4 Display Product Name (ASCII) String Descriptor Definition (tag #FCh)

The model name of the display product may be listed (optional but recommended) in the Display Product Name (ASCII) String Descriptor (tag #FCh). Up to 13 alphanumeric characters (using ASCII codes) may be used to define the model name of the display product. The data shall be sequenced such that the 1st byte (ASCII code) = the 1st character, the 2nd byte (ASCII code) = the 2nd character, etc. If there are less than 13 characters in the string, then terminate the display product name string with ASCII code '0Ah' (line feed) and pad the unused bytes in the field with ASCII code '20h' (space). Refer to Table 3.29 for information on the Display Product Name String. Refer to Appendix E for ASCII Reference Tables.

Table 3.29 – Display Product Name (ASCII) String Descriptor Block Definition

Byte #	Value	Display Product Name Definition
0 → 4	(00 00 00 FC 00)h	Display Product Name (ASCII) String Descriptor Tag Number (FCh)
5 → 17	ASCII String	Up 13 alphanumeric characters (using ASCII Codes) of a data string may be stored.

For Example: The Display Product Name String, 'XYZ_Monitor', is stored as '00h 00h 00h FCh 00h 58h 59h 5Ah 20h 4Dh 6Fh 6Eh 6Ch 74h 6Fh 72h 0Ah 20h'.

3.10.3.5 Color Point Descriptor Definition (tag #FBh)

Chromaticity coordinates (x, y) for up to two additional sets (see Section 3.7) of white points may be stored in the Color Point Descriptor (Tag # FBh). In addition, GAMMAs associated with each white point may also be defined. The color point definition is listed in Table 3.30.

Table 3.30 – Additional Color Point Descriptor Definition

Byte #	Value								Color Point Descriptor Definition
0 → 4	(00 00 00 FB 00)h								Color Point Descriptor Tag Number (FBh)
5	01h → FFh								White Point Index Number (Binary)
	00h								Reserved: Do not use.
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Bit Definitions**
6	0	0	0	0	Wx1	Wx0	Wy1	Wy0	White-x, y
7	Wx9	Wx8	Wx7	Wx6	Wx5	Wx4	Wx3	Wx2	White-x
8	Wy9	Wy8	Wy7	Wy6	Wy5	Wy4	Wy3	Wy2	White-y
9	00h → FEh								Value Stored = (GAMMA × 100) - 100 Range is 1.00 → 3.54
	FFh								GAMMA Value is not defined here. Then GAMMA data shall be stored in an EXTENSION Block; for example, DI-EXT
10	02h → FFh								White Point Index Number (Binary)
	00h								Bytes 11 to 14 are reserved – set to '00h'
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Bit Definitions**
11	0	0	0	0	Wx1	Wx0	Wy1	Wy0	White-x, y
12	Wx9	Wx8	Wx7	Wx6	Wx5	Wx4	Wx3	Wx2	White-x
13	Wy9	Wy8	Wy7	Wy6	Wy5	Wy4	Wy3	Wy2	White-y
14	00h → FEh								Value Stored = (GAMMA × 100) - 100 Range is 1.00 → 3.54
	FFh								GAMMA Value is not defined here Then GAMMA data shall be stored in an EXTENSION Block; for example, DI-EXT
15	0Ah								Line Feed - (All other values are reserved)

16, 17	20h	Space - (All other values are reserved)

Two sets of white point values may be stored. The white point chromaticity coordinates (x, y) shall be expressed as fractional numbers, accurate to the thousandth place. Each number shall be represented by a binary fraction, which is 10 bits in length. In this fraction a value of one for the bit immediately right of the decimal point (bit 9) represents 2 raised to the -1 power. A value of 1 in the right most bit (bit 0) represents a value of 2 raised to the -10 power. Add together the values for all bits set to '1'. See Table 3.31.
Some displays are capable of supporting more than one white point (color temperature). The white point index number is simply an identifier number in the range of 1 to 255. The second white point (and the white GAMMA) shall be listed first in bytes 5 → 9. A third (optional) supported white point (different index number) may be listed in bytes 10 → 14.

Table 3.31 – Ten bit Binary Fraction Representation

Bit #	Converted Back to Decimal
9	If bit 9 is set to '1', then add 2 raised to the power of -1 = 0.500
8	If bit 8 is set to '1', then add 2 raised to the power of -2 = 0.250
7	If bit 7 is set to '1', then add 2 raised to the power of -3 = 0.125
6	If bit 6 is set to '1', then add 2 raised to the power of -4 = 0.625
5	If bit 5 is set to '1', then add 2 raised to the power of -5 = 0.03125
4	If bit 4 is set to '1', then add 2 raised to the power of -6 = 0.01563
3	If bit 3 is set to '1', then add 2 raised to the power of -7 = 0.00781
2	If bit 2 is set to '1', then add 2 raised to the power of -8 = 0.00391
1	If bit 1 is set to '1', then add 2 raised to the power of -9 = 0.001953125
0	If bit 0 is set to '1', then add 2 raised to the power of -10 = 0.0009765625

In Table 3.30, the high order bits (9 → 2) shall be stored as a single byte. The low order bits (1 → 0) shall be paired with other low order bits to form the lower nibble of a byte. With this representation, all values should be accurate to +/- 0.0005 of the actual value. Examples are shown in Table 3.32.

Table 3.32 – Ten bit Binary Fraction Representation

Actual Value	Binary value	Converted Back to Decimal
0.610	1001110001	0.6103516
0.307	0100111010	0.3066406
0.150	0010011010	0.1503906

The display transfer characteristic, referred to as GAMMA, is stored in a 1-byte field capable of representing GAMMA values in the range of 1.00 to 3.54. The integer value stored is determined by the formula:

$$\text{Value stored} = (\text{GAMMA} \times 100) - 100$$

For example, a GAMMA value of 2.2 would be represented as 120 decimal (78h).

3.10.3.6 Standard Timing Identifier Definition (tag #FAh)

Six additional Standard Timings may be listed as a display descriptor (tag #FAh). The definition is shown in Table 3.33. The two byte codes (for each Standard Timing) are defined in Section 3.9.

Table 3.33 – Standard Timings (#9 to #14) Identifier Definitions

Byte #	Value	Standard Timing Identifier Definition
0 → 4	(00 00 00 FA 00)h	Standard Timing Identifier Tag Number (FAh)
5	00h → FFh	Standard Timing Identification 9
6	00h → FFh	
7	00h → FFh	Standard Timing Identification 10
8	00h → FFh	
9	00h → FFh	Standard Timing Identification 11
10	00h → FFh	
11	00h → FFh	Standard Timing Identification 12
12	00h → FFh	
13	00h → FFh	Standard Timing Identification 13
14	00h → FFh	
15	00h → FFh	Standard Timing Identification 14
16	00h → FFh	
17	0Ah	Line Feed (All other values are reserved)

Notes for Table 3.33:

1. Refer to Section 3.9 for the definition of the 2 byte standard timing identification codes.
2. It is permissible to redefine more than one 18 byte data block as Standard Timing Identifiers.
3. Additional Standard Timings may be stored in an extension block. Refer to VESA VTB-EXT Standard for more information.

3.10.3.7 Color Management Data Definition (tag #F9h)

A shorthand method of defining color management data may be listed in the Color Management Data Descriptor (Tag #F9h). This requires the storage of the Display Color Management polynomial coefficients. The polynomial coefficients shall be stored as 2 byte codes (16 bits total) --- Least Significant Byte (LSB) is stored first. Refer to Table 3.34.

Table 3.34 – Color Management Data Descriptor Definition

Byte #	Value	Color Management Data Descriptor Definitions
0 → 4	(00 00 00 F9 00)h	Color Management Data Descriptor Tag Number (F9h)
5	03h	Version Number: Set to 03h. (All other values are reserved)
6	00h → FFh	Red a_3 Least Significant Byte (LSB)
7	00h → FFh	Red a_3 Most Significant Byte (MSB)
8	00h → FFh	Red a_2 LSB
9	00h → FFh	Red a_2 MSB
10	00h → FFh	Green a_3 LSB
11	00h → FFh	Green a_3 MSB
12	00h → FFh	Green a_2 LSB
13	00h → FFh	Green a_2 MSB
14	00h → FFh	Blue a_3 LSB
15	00h → FFh	Blue a_3 MSB
16	00h → FFh	Blue a_2 LSB
17	00h → FFh	Blue a_2 MSB

Note: More information on deriving the Display Color Management polynomial coefficients is available in the VESA DCM Standard, Version 1; January 6, 2003.

3.10.3.8 CVT 3 Byte Code Descriptor Definition (tag #F8h)

Coordinated Video Timings (CVT) may be defined (optional) in the CVT 3 Byte Code Descriptor (Tag #F8h). The 3 Byte CVT Codes shall be used to define video timing modes that include horizontal and vertical pixel formats that are not defined in the VESA DMT, Version 1.0, Revision 10 or later. The CVT 3 Byte Code Descriptor section may be divided to support up to 4 timing sub-blocks - each is 3 bytes long (12 bytes total). Unused bytes shall be padded with 00h. Table 3.35 provides a description of the 3 byte CVT codes. Refer to VESA CVT Standard, Version 1.1, September 10, 2003 for more information on CVT definitions. Refer to VESA VTB-EXT Standard for more information on CVT 3 Byte Codes.

Table 3.35 – CVT 3 Byte Code Descriptor Definition

Byte #	Value	CVT 3 Byte Code Descriptor Definition
0 → 4	(00 00 00 F8 00)h	CVT 3 Byte Code Descriptor Tag Number (F8h)
5	01h	Version Number (All other values are reserved)
6 → 8	**CVT 3 Byte Code Descriptor with the #1 (Highest) Priority**	
6	**7 6 5 4 3 2 1 0**	**Eight Least Significant Bits (Bit Definitions):**
		12 Bit Value Stored = [(Addressable Lines per Field ÷ 2) – 1]
	n n n n n n n n	8 least significant bits of 12 bit Addressable Lines
	0 0 0 0 0 0 0 0	00h is Reserved: Do not use.
7	**7 6 5 4**	**Four Most Significant Bits (Bit Definitions):**
	n n n n _ _ _ _	4 most significant bits of 12 bit Addressable Lines
	3 2	**Aspect Ratio:**
	0 0	4 : 3 AR
	0 1	16 : 9 AR
	1 0	16 : 10 AR
	1 1	15 : 9 AR
	1 0	**Reserved Bits:**
	0 0	Bits 1, 0 shall be set to '00'. All other values shall not be used.
8	**7**	**Reserved Bit:**
	0	Bit 7 shall be set to '0'. The value '1' shall not be used.
	6 5	**Preferred Vertical Rate:**
	0 0	50 Hz
	0 1	60 Hz
	1 0	75 Hz
	1 1	85 Hz
	4 3 2 1 0	**Supported Vertical Rate and Blanking Style**
	1	50 Hz with standard blanking (CRT style) is supported
	1	60 Hz with standard blanking (CRT style) is supported
	1	75 Hz with standard blanking (CRT style) is supported
	1	85 Hz with standard blanking (CRT style) is supported
	1	60 Hz with reduced blanking (as per CVT Standard) is supported
9 → 11	**CVT 3 Byte Code Descriptor with the #2 Priority**	
	(00 00 00)h	If not defined then enter (00 00 00)h.
9	●●●	Refer to Byte 6 above
10	●●●	Refer to Byte 7 above
11	●●●	Refer to Byte 8 above
12 → 14	**CVT 3 Byte Code Descriptor with the #3 Priority**	
	(00 00 00)h	If not defined then enter (00 00 00)h.
12	●●●	Refer to Byte 6 above
13	●●●	Refer to Byte 7 above
14	●●●	Refer to Byte 8 above
15 → 17	**CVT 3 Byte Code Descriptor with the #4 (Lowest) Priority**	
	(00 00 00)h	If not defined then enter (00 00 00)h.
15	●●●	Refer to Byte 6 above
16	●●●	Refer to Byte 7 above
17	●●●	Refer to Byte 8 above

Notes for Table 3.35:

1. The highest priority CVT 3 byte codes (listed in the CVT 3 Byte Code Descriptor) shall be stored in the first CVT descriptor block (bytes 6, 7 & 8). The lowest priority CVT format shall be stored in the last CVT descriptor block (bytes 15, 16 & 17).

2. Together the number of "Addressable Lines per Field" and the aspect ratio determine the pixel format.
3. Addressable vertical line count is used instead of addressable horizontal pixel count due to the following:
   3.1 Using vertical line count enables a compact way of expressing multiple aspect ratios. For example a fixed format 16 : 9 AR display can center and display 4 : 3 AR and 16 : 10 AR timing which have the same number of addressable vertical lines without the need for scaling.
   3.2 Due to cell width rounding of the horizontal resolution, it may not be possible to always accurately determine the correct number of addressable vertical lines. For example: 1360x768 is a recognized 16 : 9 AR format. If the vertical resolution is calculated using the horizontal resolution a value of 765 is obtained, whereas using the vertical resolution and rounding to nearest cell width gives 1360.

The addressable **horizontal resolution** (**H**Add) is extracted by:

HAdd = 8 × {ROUNDDOWN [(**V**Add × Aspect Ratio) ÷ 8]}

Where: Aspect Ratio = 4 : 3, 16 : 9 or 16 : 10 (as specified in 3-byte CVT descriptor block)
ROUNDDOWN function rounds down to the nearest integer

Note: Timing that does not obey this rule is not CVT compliant.

4. Each 3-byte CVT descriptor block allows the display to signal support for a single display format defined by the addressable vertical line count and aspect ratio. Within that block it is possible to indicate all CVT refresh rates supported at that format. The vertical refresh rates that may be supported include: 50Hz, 60Hz, 75Hz and 85Hz and 60Hz (Reduced Blanking).
5. Any coordinated video timing outside of the monitor range limits (defined in BASE EDID) may cause the display to enter a self-protection mode (Out of Range). The host shall always verify that an intended video timing (listed in BASE EDID) falls within the display range limits before the timing is applied to the display.
6. The 'Preferred Field Rate' declares one of the 'Supported Field Rates' as preferred for the given format.
7. A Preference for 60Hz designates either 60Hz standard blanking or reduced blanking, whichever is supported. If both are supported, then reduced blanking shall be preferred. The 'Preferred Field Rate' (listed in Bits 5 & 6, Byte 8) shall also be listed in the 'Supported Field Rate' section (listed in Bits 0 → 4, Byte 8).

3.10.3.9 Established Timings III Descriptor Definition (tag #F7h)

Table 3.36 defines the Established Timings III Descriptor. Support for Established Timings III is optional. Established Timings III lists those Display Monitor Timings (DMTs) are defined in the VESA Monitor Timing Standard but are not included in Established Timings I or Established Timings II (refer to Table 3.18 in Section 3.8). Note that Established Timings III is a bit set table of supported DMTs and cannot define the video timing priority (order of importance).

Table 3.36 – Established Timings III Descriptor Definition

Byte #	Value								Established Timings III Support Definitions
0 → 4	(00 00 00 F7 00)h								Established Timings III Descriptor Tag Number (F7h)
5	0Ah								Revision Number (All other values are reserved)
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Bit Definitions:**
6	1	_	_	_	_	_	_	_	640 x 350 @ 85 Hz
	_	1	_	_	_	_	_	_	640 x 400 @ 85 Hz
	_	_	1	_	_	_	_	_	720 x 400 @ 85 Hz
	_	_	_	1	_	_	_	_	640 x 480 @ 85 Hz
	_	_	_	_	1	_	_	_	848 x 480 @ 60 Hz
	_	_	_	_	_	1	_	_	800 x 600 @ 85 Hz
	_	_	_	_	_	_	1	_	1024 x 768 @ 85 Hz
	_	_	_	_	_	_	_	1	1152 x 864 @ 75 Hz
7	1	_	_	_	_	_	_	_	1280 x 768 @ 60 Hz (RB) Note: (RB) means reduced blanking
	_	1	_	_	_	_	_	_	1280 x 768 @ 60 Hz
	_	_	1	_	_	_	_	_	1280 x 768 @ 75 Hz
	_	_	_	1	_	_	_	_	1280 x 768 @ 85 Hz
	_	_	_	_	1	_	_	_	1280 x 960 @ 60 Hz
	_	_	_	_	_	1	_	_	1280 x 960 @ 85 Hz
	_	_	_	_	_	_	1	_	1280 x 1024 @ 60 Hz
	_	_	_	_	_	_	_	1	1280 x 1024 @ 85 Hz
8	1	_	_	_	_	_	_	_	1360 x 768 @ 60 Hz
	_	1	_	_	_	_	_	_	1440 x 900 @ 60 Hz (RB)
	_	_	1	_	_	_	_	_	1440 x 900 @ 60 Hz
	_	_	_	1	_	_	_	_	1440 x 900 @ 75 Hz
	_	_	_	_	1	_	_	_	1440 x 900 @ 85 Hz
	_	_	_	_	_	1	_	_	1400 x 1050 @ 60 Hz (RB)
	_	_	_	_	_	_	1	_	1400 x 1050 @ 60 Hz
	_	_	_	_	_	_	_	1	1400 x 1050 @ 75 Hz
9	1	_	_	_	_	_	_	_	1400 x 1050 @ 85 Hz
	_	1	_	_	_	_	_	_	1680 x 1050 @ 60 Hz (RB)
	_	_	1	_	_	_	_	_	1680 x 1050 @ 60 Hz
	_	_	_	1	_	_	_	_	1680 x 1050 @ 75 Hz
	_	_	_	_	1	_	_	_	1680 x 1050 @ 85 Hz
	_	_	_	_	_	1	_	_	1600 x 1200 @ 60 Hz
	_	_	_	_	_	_	1	_	1600 x 1200 @ 65 Hz
	_	_	_	_	_	_	_	1	1600 x 1200 @ 70 Hz
10	1	_	_	_	_	_	_	_	1600 x 1200 @ 75 Hz
	_	1	_	_	_	_	_	_	1600 x 1200 @ 85 Hz
	_	_	1	_	_	_	_	_	1792 x 1344 @ 60 Hz
	_	_	_	1	_	_	_	_	1792 x 1344 @ 75 Hz
	_	_	_	_	1	_	_	_	1856 x 1392 @ 60 Hz
	_	_	_	_	_	1	_	_	1856 x 1392 @ 75 Hz
	_	_	_	_	_	_	1	_	1920 x 1200 @ 60 Hz (RB)
	_	_	_	_	_	_	_	1	1920 x 1200 @ 60 Hz
11	1	_	_	_	0	0	0	0	1920 x 1200 @ 75 Hz
	_	1	_	_	0	0	0	0	1920 x 1200 @ 85 Hz
	_	_	1	_	0	0	0	0	1920 x 1440 @ 60 Hz
	_	_	_	1	0	0	0	0	1920 x 1440 @ 75 Hz
	_	_	_	_	0	0	0	0	Reserved Bits: Shall be set to '0000'.
12 → 17	00h								Reserved Byte: Shall be set to '00h'.

Notes for Table 3.36:

1. Support for the DMTs listed in Table 3.36 is indicated by setting the appropriate bit to '1'. DMTs that are not supported are indicated by a '0'.
2. All timings listed Table 3.36 include normal blanking except those timings that are label as reduced blanking (RB).
3. For more information on refer to the newest release of the VESA DMT.

3.10.3.10 Unused – Reserved Data Tag Number (Tags #11h to #F6h)

Data Tag Numbers (#11h to #F6h) are currently undefined and are reserved (they shall not be used). In a future revision to the E-EDID Standard, VESA may define some of these data tag numbers as new descriptor blocks.

Table 3.37 – Unused Reserved Data Tag Numbers

Byte #	Value	Reserved Data Tag Number Definition
3	11h → F6h	Reserved Data Tag Numbers: Do Not Use

3.10.3.11 Dummy Descriptor Definition (Tag #10h)

The Dummy Descriptor (Tag #10h) shall be used to indicate that the descriptor space is unused. The first 5 bytes are defined in table 3.23. Table 3.38 provides a description of the Dummy Descriptor.

Table 3.38 – Dummy Descriptor Definition

Byte #	Value	Dummy Descriptor Definition
0 → 4	(00 00 00 10 00)h	Dummy Descriptor Tag Number (10h)
5 → 17	00h	All Bytes filled with '00h'
	01h → FFh	Reserved: Shall Not Be Used.

3.10.3.12 Manufacturer Specified Data Tag Numbers (Tags #00h to #0Fh)

Data Tag Numbers (#00h to #0Fh) are reserved for manufacturer specific descriptor definitions. Manufacturers may use these data tag numbers to define custom descriptors. However, manufacturers shall use the first 5 bytes as defined in Table 3.23. Table 3.39 provides a description of the Manufacturer Specified Data Descriptor.

Table 3.39 – Manufacturer Specified Data Descriptor Definition

Byte #	Value	Manufacturer Specified Data Descriptor Definition
0 → 4	(00 00 00 nn 00)h	Manufacturer Specified Data Tag Numbers (nn = 00h → 0Fh)
5 → 17	00h → FFh	Manufacturer specifies the data stored in Bytes 5 → 17

3.11 EXTENSION Flag and Checksum

The EXTENSION Flag and Checksum are required elements in EDID data structure version 1, revision 4. They are defined in Table 3.40.

Table 3.40 - EXTENSION Flag and Checksum

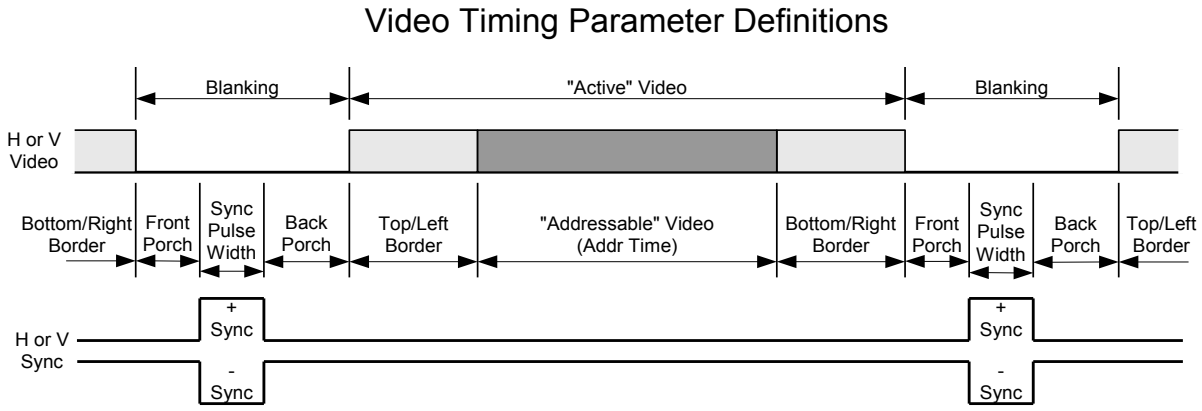
Address	Value	EXTENSION Flag & Checksum Definitions
7Eh	00h → FFh	EXTENSION Flag:
7Fh	00h → FFh	Checksum:

Notes for Table 3.40:

1. The EXTENSION Flag contains the number of EXTENSION Blocks (including optional Block Map/s) that follow the BASE EDID. Range is 0 (00h) to 255 (FFh).
2. The Checksum Byte (at address **7Fh**) shall contain a value such that a checksum of the entire 128-byte BASE EDID equals 00h.
3. The host (source) shall perform checksum error checking by adding (using modulo 256) all 128 hexadecimal bytes in the BASE EDID. If the result of the addition is '00h', then the EDID contents are probably valid.

3.12 Note Regarding Borders

This section is included to provide a clear definition of the video timing parameters listed in Table 3.22. This section also provides a frame of reference for the use of borders in detailed timings. The use of borders goes back to the early days of the PC industry (CGA, EGA, VGA, etc.). Today, borders are not in common use on personal computers. There are exceptions, for example, a widescreen (letterbox) video format in a 4 : 3 AR frame (e.g. DVD).



Definitions of Terms:

♦ Horizontal Addressable Video → The time between the end of the Left Border and the beginning of the Right Border

♦ Horizontal Blanking → The time between the end of the Right Border and the beginning of the Left Border --- includes the Horizontal Front Porch time, the Horizontal Sync Pulse Width time and the Horizontal Back Porch time

♦ Horizontal Front Porch → The time between the end of the Right Border and the beginning of the Horizontal Sync Pulse

♦ Horizontal Left Border → The time between the end of the Horizontal Blanking period and the beginning of the Horizontal Addressable Video region

♦ Horizontal Right Border → The time between the end of the Horizontal Addressable Video region and the beginning of the Horizontal Blanking period

♦ Horizontal Sync Pulse Width → The time between the end of the Horizontal Front Porch and the beginning of the Horizontal Back Porch

♦ Horizontal Back Porch → The time between the end of the Horizontal Sync Pulse and the beginning of the Left Border

♦ Horizontal Active Video → The sum of the Horizontal Left Border time, the Horizontal Addressable Video time and the Horizontal Right Border time

♦ Vertical Addressable Video → The time between the end of the Top Border and the beginning of the Bottom Border

♦ Vertical Blanking → The time between the end of the Bottom Border and the beginning of the Top Border --- includes the Vertical Front Porch time, the Vertical Sync Pulse Width time and the Vertical Back Porch time
♦ Vertical Front Porch → The time between the end of the Bottom Border and the beginning of the Vertical Sync Pulse
♦ Vertical Top Border → The time between the end of the Vertical Blanking period and the beginning of the Vertical Addressable Video region
♦ Vertical Bottom Border → The time between the end of the Vertical Addressable Video region and the beginning of the Vertical Blanking period
♦ Vertical Sync Pulse Width → The time between the end of the Vertical Front Porch and the beginning of the Vertical Back Porch
♦ Vertical Back Porch → The time between the end of the Vertical Sync Pulse and the beginning of the Top Border
♦ Vertical Active Video → The sum of the Vertical Top Border time, the Vertical Addressable Video time and the Vertical Bottom Border time

Some Additional Comments:
Both the horizontal and vertical border sizes are for one side only. (i.e. the actual number of pixels or lines taken up by both borders is twice the value listed in Table 3.21)
Borders are assumed to be symmetric for the detail timing block definition defined in Table 3.21. This is not true in the VESA DMT timing definitions.

4. EDID Extensions

Extensions to the base 128-byte EDID structure (block 0) are defined in separate VESA Standard documents.

At the time that this standard was written, the following extensions were in existence. Refer to the individual standards or specifications for more information:

- CEA-861 Series Timing Extension
- Video Timing Block Extension (VTB-EXT)
- Display Information Extension (DI-EXT)
- Localized String Extension (LS-EXT)
- Digital Packet Video Link Extension (DPVL-EXT)

5. Timing Information Priority Order

The BASE EDID data structure may contain four different types of discrete timing mode information, Established, Standard, Preferred and Detailed. There may also be information required to support GTF and/or CVT compliant displays.
The display EDID data shall be defined with the understanding that the host shall evaluate and support the timing modes in the following order:

Table 5.1 – E-EDID Timing Mode Priority

PRIORITY	Locations of All Timing Modes listed in BASE EDID and EXTENSIONS
1	The 'Preferred Timing Mode' as defined in BASE EDID. See Note 2.
2	Other 'Detailed Timing Modes' in the order listed in BASE EDID. See Note 3.
3	Any additional 'Detailed Timing Modes' (priority is in the order listed) in optional EXTENSION Blocks to the BASE EDID --- See Note 4.
4	Any optional 3 Byte CVT Codes (defined in optional Display Descriptors) listed in BASE EDID or an optional Extension Block. See Note 5.
5	'Standard Timings' listed in BASE EDID and in optional EXTENSION Blocks. See Note 6.
6	Additional Timing Mode Information: Established Timings I, II & III, Default GTF, GTF Secondary Curve & CVT. See Note 7.
7	BASE VIDEO MODE (Default VGA). See Note 8.

Notes for Table 5.1:

1) The expression "Priority is in the order listed" means that the timing mode nearest to the lowest address of the EDID structure (BASE or EXTENSION) in which the timing is contained has the highest priority, the timing at the second lowest address has the second highest priority, etc.
2) The first 18 Byte Descriptor Block (addresses **36h → 47h**) shall contain the "Preferred Timing Mode (PTM)" - the PTM has the highest priority. For more information, refer to Section 3.10.
3) Other 'Detailed Timing Modes' refers to the Detailed Timings stored in the Second (addresses **48h → 59h**), Third (addresses **5Ah → 6Bh**) and Fourth (addresses **6Ch → 7Dh**) 18 Byte Descriptors in BASE EDID. 18 Byte Descriptors may contain Display Descriptors. Some of these Display Descriptors may contain video timing information such as:
   3.1) Display Range Limits (Tag #FDh) with default GTF support, GTF Secondary Curve support or CVT support. For more information, refer to Section 3.10.3
   3.2) Standard Timings 9 → 14 (Tag #FAh). For more information, refer to Section 3.10.3.6
   3.3) 3 Byte CVT Codes (Tag #F8h). For more information, refer to Section 3.10.3.8

Detailed Timings have a higher priority compared to the timing definitions listed above (3.1 → 3.3) and the Detailed Timings are listed (in BASE EDID) in the order of importance. Timing priorities for the timing definitions listed above (3.1 → 3.3) are defined in one or more of the following notes.

4) Any additional 'Detailed Timing Modes' (listed in 18 Byte Descriptor Blocks) defined in optional EXTENSION Blocks are next in the priority order list. The priority order is in the order listed. Optional EXTENSION Blocks may include: VTB-EXT, CEA861, etc. If the standard that defines the contents of the EXTENSION Block includes a priority order definition that is in conflict, then the EXTENSION Block Standard takes precedence.
5) The next timing mode definition in the priority order list is the optional 3 Byte CVT Codes. The 3 Byte CVT Codes shall be used to define video timing modes that include horizontal and vertical pixel formats that are not defined in the VESA DMT. The 3 Byte CVT Codes may be defined in Display Descriptors which can be stored in BASE EDID or optional EXTENSION Blocks (for example: VTB-EXT, etc.). The priority order of the 3 Byte CVT Codes is in the order listed (first the BASE EDID followed by the EXTENSION Block). If the standard that defines the contents of the EXTENSION Block includes a priority order definition that is in conflict, then the EXTENSION Block Standard takes precedence.
6) Standard Timings (using 2 byte codes) are next in the priority order list. Up to 8 Standard Timings may be listed at addresses **26h → 35h** in the BASE EDID (Block 0) --- for more information, refer to section 3.9. If more than 8 Standard Timings are required, then up to six (9 → 14) additional Standard Timings may be listed in the Standard Timing Display Descriptor (Tag #FAh). The Standard Timing Display Descriptor may be located in the BASE EDID or in an optional EXTENSION Block (for example: VTB-EXT). For more information, refer to Section 3.10.3.6. If more than 14 Standard Timings are required, then multiple Standard Timing Display Descriptors may be used. If the standard that defines the contents of the EXTENSION Block includes a priority order definition that is in conflict, then the EXTENSION Block Standard takes precedence.
7) Additional Timing Mode Information includes Established Timings I & II & III, Default GTF, GTF Secondary Curve and CVT.
   7.1) Established Timings are bit set data fields that indicate the display's support for various DMTs defined in VESA DMT Version 1.0, Revision 10; October 29, 2004. Established Timings cannot define a priority order. Established Timings I & II are listed in BASE EDID at addresses **23h** & **24h**. For more information, refer to Section 3.8. Established Timings III is defined in an optional Display Descriptor (Tag #F7h). This optional Display Descriptor may be defined in BASE EDID or in an EXTENSION Block. A source may use Established Timings I, II & III to define a list of video timing modes that are supported by the display. The source cannot determine a priority order for these video timing modes.
   7.2) VESA does not recommend using the Generalized Timing Formula (GTF- using default parameters or secondary curve) for new designs. VESA recommends using CVT. Refer to Section 3.10.3.3.
8) The BASE Video Mode for Windows based Personal Computers is 640x480 @ 60 Hz (VGA). Note that some computer manufacturers (not Windows-based) have elected to define the BASE Video Mode to be some other video timing mode (not VGA).

6. APPENDIX A - Sample EDIDs

Appendix A includes 3 sample EDID data structures which are based on the E-EDID Standard Release A, Revision 2 using the version 1, revision 4 data structure definitions. These examples include: an IT desktop display; a DTV display; and a display that supports both PC and CE timing modes. These are examples only and do not represent any particular product from any particular manufacturer.

6.1 EXAMPLE 1: Sample BASE EDID (Block 0) for an LCD Desktop IT Display

Example 1 is a sample base EDID (block 0) data structure a typical LCD Desktop Display that supports PC timing modes. The following is a list of the main features:
1. 21" LCD Display (4 : 3 aspect ratio) built by the ABC Monitor Company --- Model Name is "ABC LCD21".
2. The Native Format of the display device is 1600x1200@60Hz (PC timing).
3. Preferred Mode is 1600x1200@60Hz (PC timing) using a VGA video input.
4. Supports several PC video timing modes.
5. This display is not sRGB compliant.
6. Display supports DPM power savings mode.
7. Supports CVT - supports continuous frequency inputs -Horizontal Frequency: 30 ~ 110 kHz; Vertical Frequency: 50 ~ 90 Hz.
8. Sample data structure includes: a preferred timing mode; a monitor range limits descriptor with CVT support information; established timings III; and a model name descriptor.

Address /Offset	Value HEX	Function Description	Value BIN	Value DEC	Notes
BASE EDID (Block 0)					
00	00	╦ Header:	00000000	0	See Section 3.3
01	FF	╠	11111111	255	
02	FF	╠	11111111	255	
03	FF	╠	11111111	255	
04	FF	╠	11111111	255	
05	FF	╠	11111111	255	
06	FF	╠	11111111	255	
07	00	╚	00000000	0	
08	04	╦ "ABC" – ISA PNPID	00000100	4	See Section 3.4.1
09	43	╚ Manufacturer's Code Name	01000011	67	
0A	06	╦ "F206" – ID Product Code	00000110	6	See Section 3.4.2
0B	F2	╚	11110010	242	
0C	01	╦ "00000001" – ID Serial Number	00000001	1	See Section 3.4.3
0D	00	╠	00000000	0	
0E	00	╠	00000000	0	
0F	00	╚	00000000	0	
10	01	= 1st Week of Manufacture	00000001	1	See Section 3.4.4
11	11	= "2007"-Year of Manufacture	00010001	17	
12	01	= "1" EDID Version Number	00000001	1	See Section 3.5
13	04	= "4" EDID Revision Number	00000100	4	

Address /Offset	Value HEX	Function Description	Value BIN	Value DEC	Notes
14	0F	Video Input Definition 7. Analog Video Input, 6-5. 0.700, 0.300 (1.000 Vp-p), 4. Blank Level = Black Level, 3. Separate Syncs is supported, 2. Composite Sync is supported, 1. Sync on Green is supported, 0. Vsync Serration is supported.	00001111	15	See Section 3.6.1
15	2B	Max Hor. Image Size is 43 cm.	00101011	43	See Section 3.6.2
16	20	Max Ver. Image Size is 32 cm.	00010000	32	
17	78	Display Gamma is 2.2	01111000	120	See Section 3.6.3
18	2B	Feature Support Byte: 7. Standby is not supported, 6. Suspend is not supported, 5. Active Off is supported, 4-3. Display Type is RGB Color, 2. sRGB is not supported, 1. Preferred Timing Mode includes Native Pixel Format, 0. Display is Continuous Frequency.	00101011	43	See Section 3.6.4
19	9C	Display x,y	10011100	156	See Section 3.7
1A	68	Chromaticity Coordinates:	01101000	104	
1B	A0	Red x is 0.627	10100000	160	
1C	57	Red y is 0.341	01010111	87	
1D	4A	Green x is 0.292	01001010	74	
1E	9B	Green y is 0.605	10011011	155	
1F	26	Blue x is 0.149	00100110	38	
20	12	Blue y is 0.072	00010010	18	
21	48	White x is 0.283	01001000	72	
22	4C	White y is 0.297	01001100	76	
23	FF	Supported Established Timings I include: 720x400@70Hz, 720x400@88Hz, 640x480@60Hz, 640x480@67Hz, 640x480@72Hz, 640x480@75Hz, 800x600@56Hz 800x600@60Hz	11111111	255	See Section 3.8
24	FF	Supported Established Timings II include 800x600@72Hz, 800x600@75Hz, 832x624@75Hz, 1024x768@87Hz (I), 1024x768@60Hz, 1024x768@70Hz, 1024x768@75Hz, 1280x1024@75Hz	11111111	255	

Address /Offset	Value HEX	Function Description	Value BIN	Value DEC	Notes
25	80	Supported Manufacturer's Timings include: 1152x870@75Hz	10000000	128	See Section 3.8
		Standard Timings include:			See Section 3.9
26	A9	1600x1200@85Hz,	10101001	169	
27	59		01011001	89	
28	A9	1600x1200@75Hz,	10101001	169	
29	4F		01001111	79	
2A	A9	1600x1200@70Hz,	10101001	169	
2B	4A		01001010	74	
2C	A9	1600x1200@65Hz,	10101001	169	
2D	45		01000101	69	
2E	81	1280x1024@85Hz,	10000001	129	
2F	99		10011001	153	
30	81	1280x1024@60Hz,	10000001	129	
31	80		10000000	128	
32	61	1024x768@85Hz,	01100001	97	
33	59		01011001	89	
34	45	800x600@85Hz,	01000101	69	
35	59		01011001	89	
		First 18 Byte Data Block:			See Section 3.10.2
36	48	Pixel Clock	01001000	72	Preferred Timing Mode
37	3F	is 162.000 MHz.	00111111	63	is 1600x1200@60Hz.
38	40	Horizontal Addressable Video	01000000	64	(per the VESA
39	30	is 1600 pixels. Horizontal	00110000	48	DMT Standard)
3A	62	Blanking is 560 pixels.	01100010	98	
3B	B0	Vertical Addressable Video is	10110000	176	
3C	32	1200 lines. Vertical Blanking	00110010	50	
3D	40	is 50 lines.	01000000	64	
3E	40	Horizontal Front Porch is 64 pixels.	01000000	64	
3F	C0	Horizontal Sync Pulse Width is 192 pix.	11000000	192	
40	13	Vertical Front Porch is 1 line.	00010011	19	
41	00	Vertical Sync Pulse Width is 3 lines	00000000	0	
42	AB	Horizontal Addressable Image Size	10101011	171	
43	40	is 427 mm. Vertical Addressable	01000000	64	
44	11	Image Size is 320 mm.	00010001	17	
45	00	Horizontal Border Size is 0 pixels.	00000000	0	
46	00	Vertical Border Size is 0 lines.	00000000	0	
47	1E	Timing is Non-Interlaced Video, Stereo Video is not Support, Digital Separate Syncs are required.	00011110	30	

Address /Offset	Value HEX	Function Description	Value BIN	Value DEC	Notes
		Second 18 Byte Data Block:			See Section 3.10.3.3
48	00		00000000	0	& Section 3.10.3.3.2
49	00		00000000	0	Display Range Limits
4A	00		00000000	0	Descriptor With CVT
4B	FD	= Display Range Limits Block Tag	11111101	253	Support Information
4C	00	= Horiz. & Vert. Rate Offsets are zero.	00000000	0	
4D	32	= Minimum Vertical Freq = 50 Hz	00110010	50	
4E	5A	= Maximum Vertical Freq = 90 Hz	01011010	90	
4F	1E	= Minimum Horizontal Freq = 30 KHz	00011110	30	
50	6E	= Maximum Horizontal Freq = 110 KHz	01101110	110	
51	17	= Maximum Pixel Clock Freq = 230 MHz	00010111	23	
52	04	= Begin CVT Support Information:	00000100	4	
53	11	= Compatible with CVT Version 1.1	00010001	17	
54	00	= Maximum Pixel Clock Frequency remains at 230 MHz.	00000000	0	
55	C8	= Maximum Active Pixels per Line is 1600.	11001000	200	
56	90	Supported Aspect Ratios include: 4 : 3 AR, 5 : 4 AR	10010000	144	
57	00	Preferred Aspect Ratio is 4:3, Standard CVT Blanking is supported.	00000000	0	
58	50	H. & V. Stretch are supported H. & V. Shrink are not supported.	01010000	80	
59	3C	= Preferred Refresh Rate is 60 Hz.	00111100	60	
		Third 18 Byte Data Block:			See Section 3.10.3.9
5A	00		00000000	0	Established Timings III
5B	00		00000000	0	Display Descriptor
5C	00		00000000	0	
5D	F7	= Established Timings III Block Tag	11110111	247	
5E	00		00000000	0	
5F	0A	= VESA DMT Standard Version #10	00001010	10	
60	F7	640x350@85Hz, 640x400@85Hz, 720x400@85Hz, 640x480@85Hz, 800x600@85Hz, 1024x768@85Hz, 1152x864@75Hz are supported.	11110111	247	
61	0F	1280x960@60Hz, 1280x960@85Hz, 1280x1024@60Hz, 1280x1024@85Hz	00001111	15	
62	03	1400x1050@60Hz (Normal Blanking), 1400x1050@75Hz are supported.	00000011	3	
63	87	1400x1050@85Hz, 1600x1200@60Hz, 1600x1200@65Hz, 1600x1200@70Hz are supported.	10000111	135	
64	C0	1600x1200@75Hz, 1600x1200@85Hz are supported.	11000000	192	

Address /Offset	Value HEX	Function Description	Value BIN	Value DEC	Notes
65	00	1920 Timings are not supported.	00000000	0	See Section 3.10.3.9
66	00	= Reserved --- set to '00h'	00000000	0	Established Timings III
67	00	= Reserved --- set to '00h'	00000000	0	Display Descriptor
68	00	= Reserved --- set to '00h'	00000000	0	
69	00	= Reserved --- set to '00h'	00000000	0	
6A	00	= Reserved --- set to '00h'	00000000	0	
6B	00	= Reserved --- set to '00h'	00000000	0	
		Fourth 18 Byte Data Block:			See Section 3.10.3.4
6C	00		00000000	0	Display Product Name
6D	00		00000000	0	(ASCII) String
6E	00		00000000	0	Descriptor
6F	FC	= Display Product Name Block Tag	11111100	252	
70	00		00000000	0	
71	41	= A	01000001	65	
72	42	= B	01000010	66	
73	43	= C	01000011	67	
74	20	= Space	00100000	32	
75	4C	= L	01001100	76	
76	43	= C	01000011	67	
77	44	= D	01000100	68	
78	32	= 2	00110010	50	
79	31	= 1	00110001	49	
7A	0A	= Line Feed	00001010	10	
7B	20	= Space	00100000	32	
7C	20	= Space	00100000	32	
7D	20	= Space	00100000	32	
7E	00	= Extension Flag	00000000	0	See Section 3.11
7F	0B	= Checksum	00001011	11	

End of example 1

6.2 EXAMPLE 2: Sample BASE EDID & CEA861 Extension for a DTV Display

Example 2 is a sample base EDID (block 0) data structure and a CEA861 Extension (block 1) for an LCD-TV display that supports only DTV timing modes. PC timing modes are not supported. This is a digital television display, not a PC monitor. The following is a list of the main features:

1. 47-inch LCD TV (16x9 – widescreen) built by the ABC Monitor Company - Model Name is "ABC LCD47w".
2. Native pixel format of the LCD panel is 1920 x 1080.
3. Preferred Timing Mode is 1920 x 1080p @ 60 Hz (DTV timing) using an HDMI-a video input.
4. PC video timing modes are not supported.
5. sRGB compliant.
6. Does not support GTF or CVT.
7. Sample data structure includes a preferred DTV timing mode, a second DTV detailed timing, a third DTV detailed timing and a model name descriptor.

Address /Offset	Value HEX	Function Description	Value BIN	Value DEC	Notes
BASE EDID (Block 0)					
00	00	Header:	00000000	0	See Section 3.3
01	FF		11111111	255	
02	FF		11111111	255	
03	FF		11111111	255	
04	FF		11111111	255	
05	FF		11111111	255	
06	FF		11111111	255	
07	00		00000000	0	
08	04	"ABC" – EISA ID	00000100	4	See Section 3.4.1
09	43	Manufacturer's Code Name	01000011	67	
0A	07	"F207" – ID Product Code	00000111	7	See Section 3.4.2
0B	F2		11110010	242	
0C	01	"00000001" – ID Serial Number	00000001	1	See Section 3.4.3
0D	00		00000000	0	
0E	00		00000000	0	
0F	00		00000000	0	
10	FF	= Model Year Flag	11111111	255	See Section 3.4.4
11	11	= "2007" is the Model Year	00010001	17	
12	01	= "1" EDID Version Number	00000001	1	See Section 3.5
13	04	= "4" EDID Revision Number	00000100	4	
14	A2	Digital Video Input using HDMI-a, 8 Bits per Primary Color	10100010	162	See Section 3.6.1
15	4F	= Aspect Ratio is 16 : 9 AR in Landscape	01001111	79	See Section 3.6.2
16	00	= Aspect Ratio (Landscape) Flag	00000000	0	
17	78	= Display Gamma is 2.20	01111000	120	See Section 3.6.3

Address /Offset	Value HEX	Function Description	Value BIN	Value DEC	Notes
18	1E	Feature Support Byte: 7. Standby is not supported 6. Suspend is not supported 5. Active Off is not supported 4-3. RGB 4:4:4, YCrCb 4:4:4 & YCrCb 4:2:2 are supported. 2. sRGB is supported 1. Preferred Timing Mode includes Native Pixel Format, 0. Display is Non-Continuous Frequency.	00011110	30	See Section 3.6.4
19	EE	Display x,y Chromaticity	11101110	238	See Section 3.7
1A	91	Coordinates:	10010001	145	
1B	A3	Red x is 0.640	10100011	163	
1C	54	Red y is 0.330	01010100	84	
1D	4C	Green x is 0.300	01001100	76	
1E	99	Green y is 0.600	10011001	153	
1F	26	Blue x is 0.150	00100110	38	
20	0F	Blue y is 0.060	00001111	15	
21	50	White x is 0.313 (D65)	01010000	80	
22	54	White y is 0.329 (D65)	01010100	84	
23	20	Supported Established Timings I include: 640x480@60Hz,	00100000	32	See Section 3.8
24	00	Established Timings II include: None Specified	00000000	0	
25	00	Manufacturer's Timings: – None Specified	00000000	0	
		Standard Timings include:			See Section 3.9
26	01	Not Specified	00000001	1	
27	01		00000001	1	
28	01	Not Specified	00000001	1	
29	01		00000001	1	
2A	01	Not Specified	00000001	1	
2B	01		00000001	1	
2C	01	Not Specified	00000001	1	
2D	01		00000001	1	
2E	01	Not Specified	00000001	1	
2F	01		00000001	1	
30	01	Not Specified	00000001	1	
31	01		00000001	1	
32	01	Not Specified	00000001	1	
33	01		00000001	1	
34	01	Not Specified	00000001	1	
35	01		00000001	1	

Address /Offset	Value HEX	Function Description	Value BIN	Value DEC	Notes
		First 18 Byte Data Block:			See Section 3.10.2
36	02	╥ Pixel Clock	00000010	2	Preferred Timing Mode
37	3A	╨ is 148.500 MHz.	00111010	58	1920x1080@60Hz
38	80	╥ Horizontal Addressable Video	10000000	128	(1080p DTV Timing)
39	18	╢ is 1920 Pixels. Horizontal	00011000	24	(CEA Format #16)
3A	71	╨ Blanking is 280 Pixels.	01111000	113	(per CEA861 Standard)
3B	38	╥ Vertical Addressable Video is	00111000	56	
3C	2D	╢ 1080 lines. Vertical Blanking	00101101	45	
3D	40	╨ is 45 lines.	01000000	64	
3E	58	╥ Horizontal Front Porch is 88 Pixels.	01011000	88	
3F	2C	╢ Horizontal Sync Pulse Width is 44.	00101100	44	
40	04	╢ Vertical Front Porch is 4 lines.	00000100	4	
41	05	╨ Vertical Sync Pulse Width is 5 lines.	00000101	5	
42	0F	╥ Horizontal Addressable Image Size	00001111	15	
43	48	╢ is 1039 mm. Vertical Addressable	01001000	72	
44	42	╨ Image Size is 584 mm.	01000010	66	
45	00	═ Horizontal Border Size is 0 pixels.	00000000	0	
46	00	═ Vertical Border Size is 0 lines.	00000000	0	
47	1E	╔ Timing is Non-Interlaced Video, ╬ Stereo Video is not Support, ╚ Digital Separate + Syncs are required.	00011110	30	
		Second 18 Byte Data Block:			See Section 3.10.2
48	01	╥ Pixel Clock	00000001	1	Detailed Timing
49	1D	╨ is 74.250 MHz.	00011101	29	Descriptor - 1920x1080
4A	80	╥ Horizontal Addressable Video	10000000	128	@60Hz Interlaced
4B	18	╢ is 1920 Pixels. Horizontal	00011000	24	(1080i DTV Timing)
4C	71	╨ Blanking is 280 Pixels.	01111000	113	(CEA Format #5)
4D	1C	╥ Vertical Addressable Video is	00011100	28	(per CEA861 Standard)
4E	16	╢ 540 lines. Vertical Blanking	00010110	22	
4F	20	╨ is 22 lines.	00100000	32	
50	58	╥ Horizontal Front Porch is 88 Pixels.	01011000	88	
51	2C	╢ Horizontal Sync Pulse Width is 44.	00101100	44	
52	25	╢ Vertical Front Porch is 2 lines.	00100101	37	
53	00	╨ Vertical Sync Pulse Width is 5 lines.	00000000	0	
54	0F	╥ Horizontal Addressable Image Size	00001111	15	
55	48	╢ is 1039 mm. Vertical Addressable	01001000	72	
56	42	╨ Image Size is 584 mm.	01000010	66	
57	00	═ Horizontal Border Size is 0 pixels.	00000000	0	
58	00	═ Vertical Border Size is 0 lines.	00000000	0	
59	9E	╔ Timing is Interlaced Video, ╬ Stereo Video is not Support, ╚ Digital Separate + Syncs are required.	10011110	158	

Address /Offset	Value HEX	Function Description	Value BIN	Value DEC	Notes
		Third 18 Byte Data Block:			See Section 3.10.2
5A	01	╥ Pixel Clock	00000001	1	Detailed Timing
5B	1D	╨ is 74.250 MHz.	00011101	29	Descriptor - 1280x720
5C	00	╥ Horizontal Addressable Video	00000000	0	@60Hz Non-Interlaced
5D	72	╢ is 1280 pixels. Horizontal	01110010	114	(720p DTV Timing)
5E	51	╨ Blanking is 370 pixels.	01010001	81	(CEA Format #4)
5F	D0	╥ Vertical Addressable Video is	11010000	208	(per CEA861 Standard)
60	1E	╢ 720 lines. Vertical Blanking	00011110	30	
61	20	╨ is 30 lines.	00100000	32	
62	6E	╥ Horizontal Front Porch is 110 pixels.	01101110	110	
63	28	╢ Horizontal Sync Pulse Width is 40 pixels	00101000	40	
64	55	╢ Vertical Front Porch is 5 lines.	01010101	85	
65	00	╨ Vertical Sync Pulse Width is 5 lines.	00000000	0	
66	0F	╥ Horizontal Addressable Image Size	11001101	205	
67	48	╢ is 1039 mm. Vertical Addressable	10110011	179	
68	42	╨ Image Size is 584 mm.	01000010	66	
69	00	═ Horizontal Border Size is 0 pixels.	00000000	0	
6A	00	═ Vertical Border Size is 0 lines.	00000000	0	
6B	1E	╔ Timing is Non-Interlaced Video, ╬ Stereo Video is not Support, ╚ Digital Separate + Syncs are required.	00011110	30	
		Fourth 18 Byte Data Block:			See Section 3.10.3.4
6C	00	Monitor Name ASCII Descriptor	00000000	0	
6D	00		00000000	0	
6E	00		00000000	0	
6F	FC	═ Monitor Name Tag	11111100	252	
70	00		00000000	0	
71	41	═ A	01000001	65	
72	42	═ B	01000010	66	
73	43	═ C	01000011	67	
74	20	═ Space	00100000	32	
75	4C	═ L	01001100	76	
76	43	═ C	01000011	67	
77	44	═ D	01000100	68	
78	34	═ 4	00110111	52	
79	37	═ 7	00110111	55	
7A	77	═ w	01110111	119	
7B	0A	═ Line Feed	00001010	10	
7C	20	═ Space	00100000	32	
7D	20	═ Space	00100000	32	
7E	01	═ Extension Flag	00000001	1	See Section 3.11
7F	CB	═ Checksum	11001011	203	

Address /Offset	Value HEX	Function Description	Value BIN	Value DEC	Notes
CEA 861 EXTENSION Block – Version 3 (Block 1)					Refer to CEA 861 Standard for definitions
80	02	CEA 861 EXTENSION Block Tag Code '02h'	00000010	2	
81	03	CEA 861 EXTENSION Block Version #3	00000011	3	
82	18	Detail Timing Descriptors start at address 9Ah	00011000	24	
83	72	Underscan is not supported. Basic Audio is supported. YCbCr 4:4:4 & YCbCr 4:2:2 are supported. Number of native formats is 2	01110010	114	
84	47	Video Data Block Tag Code is 2. Number of Short Video Descriptor Bytes is 7.	01000111	71	
85	90	1920x1080p 59.94/60 Hz 16 : 9 AR (CEA Format #16) is a supported Native Format.	10010000	144	
86	85	1920x1080i 59.94/60 Hz 16 : 9 AR (CEA Format #5) is a supported Native Format.	10000110	133	
87	04	1280x720p 59.94/60 Hz 16 : 9 AR (CEA Format #4) is a supported format.	00000100	4	
88	03	720x480p 59.94/60 Hz 16 : 9 AR (CEA Format #3) is a supported format.	00000011	3	
89	02	720x480p 59.94/60 Hz 4 : 3 AR (CEA Format #2) is a supported format.	00000010	2	
8A	07	720x480i 59.94/60 Hz 16 : 9 AR (CEA Format #7) is a supported format.	00000111	7	
8B	06	720x480i 59.94/60 Hz 4 : 3 AR (CEA Format #6) is a supported format.	00000110	6	
8C	23	Audio Data Block Tag Code is 1. Number of Short Audio Descriptor Bytes is 3.	00100011	35	
8D	09	Audio Format Tag Code is 1 --- LPCM is supported. Maximum number of audio channels is 2.	00001001	9	
8E	07	Supported Sampling Frequencies include: 48kHz; 44.1kHz & 32kHz.	00000111	7	
8F	07	Supported Sampling Bit Rates include: 24 bit; 20 bit & 16 bit.	0000111	7	
90	83	Speaker Allocation Block Tag Code is 4. Number of Speaker Allocation Descriptor Bytes is 3.	10000011	131	
91	01	Speaker Allocation is Front-Left & Front-Right.	00000001	1	
92	00	Reserved (Shall be 00h).	00000000	0	
93	00	Reserved (Shall be 00h).	00000000	0	

Address /Offset	Value HEX	Function Description	Value BIN	Value DEC	Notes
94	65	╔ Vendor Specific Data Block Tag Code ╬ is 3. Number of Vendor Specific Data ╚ Bytes is 5.	01100101	101	
95	03	╦ The 24 bit IEEE Registration Identifier	00000011	3	
96	0C	╬ is ‘000C03h’.	00001100	12	
97	00	╝	00000000	0	
98	10	╦ Vendor Specific Data is ‘1000h’.	10000000	16	
99	00	╝	00000000	0	
		Fifth 18 Byte Data Block:			Detailed Timing
9A	8E	╦ Pixel Clock	10001110	142	Descriptor – 720x480
9B	0A	╩ is 27.027 MHz.	00001010	10	@60Hz Non-Interlaced
9C	D0	╦ Horizontal Addressable Video	11010000	208	(480p, 16 : 9 AR
9D	8A	╣ is 720 pixels. Horizontal	10001010	138	DTV Timing)
9E	20	╩ Blanking is 138 pixels.	00100000	32	(CEA Format #3)
9F	E0	╦ Vertical Addressable Video is	11100000	224	(per CEA861 Standard)
A0	2D	╣ 480 lines. Vertical Blanking	00101101	45	
A1	10	╩ is 45 lines.	00010000	16	
A2	10	╦ Horizontal Front Porch is 16 pixels.	00010000	16	
A3	3E	╣ Horizontal Sync Pulse Width is 62 pixels	00111110	62	
A4	96	╣ Vertical Front Porch is 9 lines.	10010110	150	
A5	00	╩ Vertical Sync Pulse Width is 6 lines.	00000000	0	
A6	1F	╦ Displayed Image	00011111	16	
A7	09	╣ Aspect Ratio	00001001	9	
A8	00	╩ is 16 by 9.	00000000	00	
A9	00	═ Horizontal Border Size is 0 pixels.	00000000	0	
AA	00	═ Vertical Border Size is 0 lines.	00000000	0	
AB	18	╔ Timing is Interlaced Video, ╬ Stereo Video is not Support, ╚ Digital Separate □ Syncs are required.	00011000	24	
		Sixth 18 Byte Data Block:			Detailed Timing
AC	8E	╦ Pixel Clock	10001110	142	Descriptor – 720x480
AD	0A	╩ is 27.027 MHz.	00001010	10	@60Hz Non-Interlaced
AE	D0	╦ Horizontal Addressable Video	11010000	208	(480p, 4 : 3 AR
AF	8A	╣ is 720 pixels. Horizontal	10001010	138	DTV Timing)
B0	20	╩ Blanking is 138 pixels.	00100000	32	(CEA Format #2)
B1	E0	╦ Vertical Addressable Video is	11100000	224	(per CEA861 Standard)
B2	2D	╣ 480 lines. Vertical Blanking	00101101	45	
B3	10	╩ is 45 lines.	00010000	16	
B4	10	╦ Horizontal Front Porch is 16 pixels.	00010000	16	
B5	3E	╣ Horizontal Sync Pulse Width is 62 pixels	00111110	62	
B6	96	╣ Vertical Front Porch is 9 lines.	10010110	150	
B7	00	╩ Vertical Sync Pulse Width is 6 lines.	00000000	0	
B8	04	╦ Displayed Image	00000100	4	
B9	03	╣ Aspect Ratio	00000011	3	
BA	00	╩ is 4 by 3.	00000000	00	
BB	00	═ Horizontal Border Size is 0 pixels.	00000000	0	
BC	00	═ Vertical Border Size is 0 lines.	00000000	0	

Address /Offset	Value HEX	Function Description	Value BIN	Value DEC	Notes
BD	18	╔ Timing is Interlaced Video, ╬ Stereo Video is not Support, ╚ Digital Separate □ Syncs are required.	00011000	24	
		Seventh 18 Byte Data Block:			Detailed Timing
BE	8E	╦ Pixel Clock	10001110	142	Descriptor – 720x480
BF	0A	╩ is 27.027 MHz.	00001010	10	@60Hz Interlaced
C0	A0	╦ Horizontal Addressable Video	10100000	160	(480i, 16 : 9 AR
C1	14	╣ is 1440 pixels. Horizontal	00010100	20	DTV Timing)
C2	51	╩ Blanking is 276 pixels.	01010001	81	(CEA Format #7)
C3	F0	╦ Vertical Addressable Video is	11110000	240	(per CEA861 Standard)
C4	16	╣ 240 lines. Vertical Blanking	00010110	22	
C5	00	╩ is 23 lines.	00000000	0	
C6	26	╦ Horizontal Front Porch is 38 pixels.	00100110	38	
C7	7C	╣ Horizontal Sync Pulse Width is 124 pix.	01111100	124	
C8	43	╣ Vertical Front Porch is 4 lines.	01000011	67	
C9	00	╩ Vertical Sync Pulse Width is 3 lines.	00000000	0	
CA	1F	╦ Displayed Image	00011111	16	
CB	09	╣ Aspect Ratio	00001001	9	
CC	00	╩ is 16 by 9.	00000000	00	
CD	00	═ Horizontal Border Size is 0 pixels.	00000000	0	
CE	00	═ Vertical Border Size is 0 lines.	00000000	0	
CF	98	╔ Timing is Interlaced Video, ╬ Stereo Video is not Support, ╚ Digital Separate □ Syncs are required.	10011000	152	
		Eighth 18 Byte Data Block:			Detailed Timing
D0	8E	╦ Pixel Clock	10001110	142	Descriptor – 720x480
D1	0A	╩ is 27.027 MHz.	00001010	10	@60Hz Interlaced
D2	A0	╦ Horizontal Addressable Video	10100000	160	(480i, 4 : 3 AR
D3	14	╣ is 1440 pixels. Horizontal	00010100	20	DTV Timing)
D4	51	╩ Blanking is 276 pixels.	01010001	81	(CEA Format #6)
D5	F0	╦ Vertical Addressable Video is	11110000	240	(per CEA861 Standard)
D6	16	╣ 240 lines. Vertical Blanking	00010110	22	
D7	00	╩ is 23 lines.	00000000	0	
D8	26	╦ Horizontal Front Porch is 38 pixels.	00100110	38	
D9	7C	╣ Horizontal Sync Pulse Width is 124 pix.	01111100	124	
DA	43	╣ Vertical Front Porch is 4 lines.	01000011	67	
DB	00	╩ Vertical Sync Pulse Width is 3 lines.	00000000	0	
DC	04	╦ Displayed Image	00000100	4	
DD	03	╣ Aspect Ratio	00000011	3	
DE	00	╩ is 4 by 3.	00000000	00	
DF	00	═ Horizontal Border Size is 0 pixels.	00000000	0	
E0	00	═ Vertical Border Size is 0 lines.	00000000	0	
E1	98	╔ Timing is Interlaced Video, ╬ Stereo Video is not Support, ╚ Digital Separate □ Syncs are required.	10011000	152	

Address /Offset	Value HEX	Function Description	Value BIN	Value DEC	Notes
		Unused Addresses			
E2	00	= No Data	00000000	0	
E3	00	= No Data	00000000	0	
E4	00	= No Data	00000000	0	
E5	00	= No Data	00000000	0	
E6	00	= No Data	00000000	0	
E7	00	= No Data	00000000	0	
E8	00	= No Data	00000000	0	
E9	00	= No Data	00000000	0	
EA	00	= No Data	00000000	0	
EB	00	= No Data	00000000	0	
EC	00	= No Data	00000000	0	
ED	00	= No Data	00000000	0	
EE	00	= No Data	00000000	0	
EF	00	= No Data	00000000	0	
F0	00	= No Data	00000000	0	
F1	00	= No Data	00000000	0	
F2	00	= No Data	00000000	0	
F3	00	= No Data	00000000	0	
F4	00	= No Data	00000000	0	
F5	00	= No Data	00000000	0	
F6	00	= No Data	00000000	0	
F7	00	= No Data	00000000	0	
F8	00	= No Data	00000000	0	
F9	00	= No Data	00000000	0	
FA	00	= No Data	00000000	0	
FB	00	= No Data	00000000	0	
FC	00	= No Data	00000000	0	
FD	00	= No Data	00000000	0	
FE	00	= No Data	00000000	0	
FF	C9	= Checksum	10011000	152	

End of example 2

6.3 EXAMPLE 3: Sample BASE EDID & CEA861 Extension for a IT/DTV Display

Example 3 is a sample base EDID (block 0) data structure and a CEA861 Extension (block 1) for a 50-inch plasma display that supports both IT (PC) timing modes and DTV timing modes. This is a dual purpose display. The following is a list of the main features:

1. 55-inch Plasma Display (16 : 9 AR – widescreen) built by the ABC Monitor Company - Model Name is "ABC PLA55".
2. Native format of the plasma panel is 1366 by 768.
3. Preferred Mode is 1360x768@60Hz (IT timing) using an HDMI-a video input.
4. s-RGB compliant.
5. Does not support GTF or CVT.
6. Sample data structure includes: the preferred IT timing mode; a DTV detailed timing; established timings III; and a model name descriptor.

Address /Offset	Value HEX	Function Description	Value BIN	Value DEC	Notes
BASE EDID (Block 0)					
00	00	Header:	00000000	0	See Section 3.3
01	FF		11111111	255	
02	FF		11111111	255	
03	FF		11111111	255	
04	FF		11111111	255	
05	FF		11111111	255	
06	FF		11111111	255	
07	00		00000000	0	
08	04	"ABC" – EISA_ID	00000100	4	See Section 3.4.1
09	43	Manufacturer's Code Name	01000011	67	
0A	08	"F208" – ID Product Code	00001000	8	See Section 3.4.2
0B	F2		11110010	242	
0C	01	"00000001" – ID Serial Number	00000001	1	See Section 3.4.3
0D	00		00000000	0	
0E	00		00000000	0	
0F	00		00000000	0	
10	10	= Week of Manufacture is 16	00010000	16	See Section 3.4.4
11	11	= Year of Manufacture is 2007	00010001	17	
12	01	= "1" EDID Version Number	00000001	1	See Section 3.5
13	04	= "4" EDID Revision Number	00000100	4	
14	A2	Digital Video Input using HDMI-a, 8 Bits per Primary Color	10100010	162	See Section 3.6.1
15	79	= Aspect Ratio is 16 : 9 AR in Landscape	01111001	121	See Section 3.6.2
16	44	= Aspect Ratio (Landscape) Flag	01000100	68	
17	78	= Display Gamma is 2.20	01111000	120	See Section 3.6.3

Address /Offset	Value HEX	Function Description	Value BIN	Value DEC	Notes
18	1E	Feature Support Byte: 7. Standby is not supported 6. Suspend is not supported 5. Active Off is not supported 4-3. RGB 4:4:4, YCrCb 4:4:4 & YCrCb 4:2:2 are supported. 2. sRGB is supported 1. Preferred Timing Mode includes Native Pixel Format, 0. Display is Non-Continuous Frequency.	00011110	30	See Section 3.6.4
19	EE	Display x,y Chromaticity	11101110	238	See Section 3.7
1A	91	Coordinates:	10010001	145	
1B	A3	Red x is 0.640	10100011	163	
1C	54	Red y is 0.330	01010100	84	
1D	4C	Green x is 0.300	01001100	76	
1E	99	Green y is 0.600	10011001	153	
1F	26	Blue x is 0.150	00100110	38	
20	0F	Blue y is 0.060	00001111	15	
21	50	White x is 0.313 (D65)	01010000	80	
22	54	White y is 0.329 (D65)	01010100	84	
23	FF	Established Timings I include: 720x400@70Hz/88Hz; 640x480@60Hz/67Hz/72Hz/75Hz & 800x600@56Hz/60Hz	11111111	255	See Section 3.8
24	EF	Established Timings II include: 800x600@72Hz/75Hz; 832x624@75Hz; 1024x768@60Hz/70Hz/75Hz & 1280x1024@75Hz	11101111	254	
25	80	Manufacturer's Timings include: 1152x870@75Hz	10000000	128	
		Standard Timings include:			See Section 3.9
26	81	1280x1024@85Hz	10000001	129	
27	99		10011001	153	
28	81	1280x1024@60Hz	10000001	129	
29	80		10000000	128	
2A	81	1280x960@85Hz	10000001	129	
2B	59		01011001	89	
2C	81	1280x960@60Hz	10000001	129	
2D	40		01000000	64	
2E	61	1024x768@85Hz	01100001	97	
2F	59		01011001	89	
30	4B	848x480@60Hz	01001011	75	
31	C0		11000001	192	
32	45	800x600@85Hz	00100101	69	
33	59		01011001	89	
34	31	640x480@85Hz	00110001	49	
35	59		01011001	89	

Address /Offset	Value HEX	Function Description	Value BIN	Value DEC	Notes
		First 18 Byte Data Block:			See Section 3.10.2
36	66	╦ Pixel Clock	01100110	102	Preferred Timing Mode
37	21	╩ is 85.500 MHz.	00100001	33	1360x768@60Hz
38	50	╦ Horizontal Addressable Video	01010000	80	(PC Timing)
39	B0	╣ is 1360 pixels. Horizontal	10110000	176	(per VESA DMT
3A	51	╩ Blanking is 432 pixels.	01010001	81	Standard)
3B	00	╦ Vertical Addressable Video is	00000000	0	
3C	1B	╣ 768 lines. Vertical Blanking	00011011	27	
3D	30	╩ is 27 lines.	00110000	48	
3E	40	╦ Horizontal Front Porch is 64 pixels.	01000000	64	
3F	70	╣ Horizontal Sync Pulse Width is 112 pix.	01110000	112	
40	36	╣ Vertical Front Porch is 3 lines.	00110110	54	
41	00	╩ Vertical Sync Pulse Width is 6 lines.	00000000	0	
42	BE	╦ Horizontal Addressable Image Size	10111110	190	
43	AB	╣ is 1214 mm. Vertical Addressable	10101011	171	
44	42	╩ Image Size is 683 mm.	01000010	66	
45	00	═ Horizontal Border Size is 0 pixels.	00000000	0	
46	00	═ Vertical Border Size is 0 lines.	00000000	0	
47	1E	╔ Timing is Non-Interlaced Video, ╬ Stereo Video is not Support, ╚ Digital Separate + Syncs are required.	00011110	30	
		Second 18 Byte Data Block:			See Section 3.10.2
48	01	╦ Pixel Clock	01100110	102	Descriptor - 1280x720
49	1D	╩ is 74.250 MHz.	00100001	33	@60Hz Non-Interlaced
4A	00	╦ Horizontal Addressable Video	00000000	0	(720p DTV Timing)
4B	72	╣ is 1280 pixels. Horizontal	01110010	114	(CEA Format #4)
4C	51	╩ Blanking is 370 pixels.	01010001	81	(per CEA861 Standard)
4D	D0	╦ Vertical Addressable Video is	11010000	208	
4E	1E	╣ 720 lines. Vertical Blanking	00011110	30	
4F	20	╩ is 30 lines.	00100000	32	
50	6E	╦ Horizontal Front Porch is 110 pixels.	01101110	110	
51	28	╣ Horizontal Sync Pulse Width is 40 pixels	00101000	40	
52	55	╣ Vertical Front Porch is 5 lines.	01010101	85	
53	00	╩ Vertical Sync Pulse Width is 5 lines.	00000000	0	
54	BE	╦ Horizontal Addressable Image Size	10111110	190	
55	AB	╣ is 1214 mm. Vertical Addressable	10101011	171	
56	42	╩ Image Size is 683 mm.	01000010	66	
57	00	═ Horizontal Border Size is 0 pixels.	00000000	0	
58	00	═ Vertical Border Size is 0 lines.	00000000	0	
59	1E	╔ Timing is Non-Interlaced Video, ╬ Stereo Video is not Support, ╚ Digital Separate + Syncs are required.	00011110	30	
		Third 18 Byte Data Block:			See Section 3.10.3.9
5A	00	Established Timings III Descriptor	00000000	0	Established Timings III
5B	00		00000000	0	Display Descriptor
5C	00		00000000	0	
5D	F7	═ Established Timings III Block Tag	11110111	247	
5E	00		00000000	0	

Address /Offset	Value HEX	Function Description	Value BIN	Value DEC	Notes
5F	0A	= VESA DMT Standard Version #10	00001010	10	See Section 3.10.3.9 Established Timings III Display Descriptor
60	F7	640x350@85Hz, 640x400@85Hz, 720x400@85Hz, 640x480@85Hz, 800x600@85Hz, 1024x768@85Hz, 1152x864@75Hz are supported.	11110111	247	
61	0F	1280x960@60Hz, 1280x960@85Hz, 1280x1024@60Hz, 1280x1024@85Hz	00001111	15	
62	03	1400x1050@60Hz (Normal Blanking), 1400x1050@75Hz are supported.	00000011	3	
63	87	1400x1050@85Hz, 1600x1200@60Hz, 1600x1200@65Hz, 1600x1200@70Hz are supported.	10000111	135	
64	C0	1600x1200@75Hz, 1600x1200@85Hz are supported.	11000000	192	
65	00	= 1920 PC Timings are not supported.	00000000	0	
66	00	= Reserved --- set to '00h'	00000000	0	
67	00	= Reserved --- set to '00h'	00000000	0	
68	00	= Reserved --- set to '00h'	00000000	0	
69	00	= Reserved --- set to '00h'	00000000	0	
6A	00	= Reserved --- set to '00h'	00000000	0	
6B	00	= Reserved --- set to '00h'	00000000	0	
		Fourth 18 Byte Data Block:			See Section 3.10.3.4
6C	00	Monitor Name ASCII Descriptor	00000000	0	
6D	00		00000000	0	
6E	00		00000000	0	
6F	FC	= Monitor Name Tag	11111100	252	
70	00		00000000	0	
71	41	= A	01000001	65	
72	42	= B	01000010	66	
73	43	= C	01000011	67	
74	20	= Space	00100000	32	
75	50	= P	01010000	80	
76	4C	= L	01001100	76	
77	41	= A	01000001	65	
78	35	= 5	00110101	53	
79	35	= 5	00110101	53	
7A	0A	= Line Feed	00001010	10	
7B	20	= Space	00100000	32	
7C	20	= Space	00100000	32	
7D	20	= Space	00100000	32	
7E	01	= Extension Flag	00000001	1	See Section 3.11
7F	0A	= Checksum	00001010	10	

Address /Offset	Value HEX	Function Description	Value BIN	Value DEC	Notes
CEA 861 EXTENSION Block – Version 3 (Block 1)					Refer to CEA 861 Standard for definitions of the data fields contained in Block 1.
80	02	CEA 861 EXTENSION Block Tag Code '02h'	00000010	2	
81	03	CEA 861 EXTENSION Block Version #3	00000011	3	
82	17	Detail Timing Descriptors start at address 99h	00011000	24	
83	F0	Underscan is supported. Basic Audio is supported. YCbCr 4:4:4 & YCbCr 4:2:2 are supported. Number of native formats is 0	11110000	240	
84	46	Video Data Block Tag Code is 2. Number of Short Video Descriptor Bytes is 6.	01000110	70	
85	05	1920x1080i 59.94/60 Hz 16 : 9 AR (CEA Format #5) is a supported format.	00000101	5	
86	04	1280x720p 59.94/60 Hz 16 : 9 AR (CEA Format #4) is a supported format.	00000100	4	
87	03	720x480p 59.94/60 Hz 16 : 9 AR (CEA Format #3) is a supported format.	00000011	3	
88	02	720x480p 59.94/60 Hz 4 : 3 AR (CEA Format #2) is a supported format.	00000010	2	
89	07	720x480i 59.94/60 Hz 16 : 9 AR (CEA Format #7) is a supported format.	00000111	7	
8A	06	720x480i 59.94/60 Hz 4 : 3 AR (CEA Format #6) is a supported format.	00000110	6	
8B	23	Audio Data Block Tag Code is 1. Number of Short Audio Descriptor Bytes is 3.	00100011	35	
8C	09	Audio Format Tag Code is 1 --- LPCM is supported. Maximum number of audio channels is 2.	00001001	9	
8D	07	Supported Sampling Frequencies include: 48kHz; 44.1kHz & 32kHz.	00000111	7	
8E	07	Supported Sampling Bit Rates include: 24 bit; 20 bit & 16 bit.	0000111	7	
8F	83	Speaker Allocation Block Tag Code is 4. Number of Speaker Allocation Descriptor Bytes is 3.	10000011	131	
90	01	Speaker Allocation is Front-Left & Front-Right.	00000001	1	
91	00	Reserved (Shall be 00h).	00000000	0	
92	00	Reserved (Shall be 00h).	00000000	0	

Address /Offset	Value HEX	Function Description	Value BIN	Value DEC	Notes
93	65	╔ Vendor Specific Data Block Tag Code ╠ is 3. Number of Vendor Specific Data ╚ Bytes is 5.	01100101	101	
94	03	╔ The 24 bit IEEE Registration Identifier	00000011	3	
95	0C	╠ is ‘000C03h’.	00001100	12	
96	00	╝	00000000	0	
97	10	╔ Vendor Specific Data is ‘1000h’.	10000000	16	
98	00	╝	00000000	0	
		Fifth 18 Byte Data Block:			Detailed Timing
99	01	╔ Pixel Clock	00000001	1	Descriptor - 1920x1080
9A	1D	╚ is 74.250 MHz.	00011101	29	@60Hz Interlaced
9B	80	╔ Horizontal Addressable Video	10000000	128	(1080i DTV Timing)
9C	18	╢ is 1920 pixels. Horizontal	00011000	24	(CEA Format #5)
9D	71	╚ Blanking is 280 pixels.	01111000	113	(per CEA861 Standard)
9E	1C	╔ Vertical Addressable Video is	00011100	28	
9F	16	╢ 540 lines. Vertical Blanking	00010110	22	
A0	20	╚ is 22 lines.	00100000	32	
A1	58	╔ Horizontal Front Porch is 88 pixels.	01011000	88	
A2	2C	╢ Horizontal Sync Pulse Width is 44 pixels	00101100	44	
A3	25	╢ Vertical Front Porch is 2 lines.	00100101	37	
A4	00	╚ Vertical Sync Pulse Width is 5 lines.	00000000	0	
A5	0F	╔ Horizontal Addressable Image Size	00001111	15	
A6	48	╢ is 1039 mm. Vertical Addressable	01001000	72	
A7	42	╚ Image Size is 584 mm.	01000010	66	
A8	00	═ Horizontal Border Size is 0 pixels.	00000000	0	
A9	00	═ Vertical Border Size is 0 lines.	00000000	0	
AA	9E	╔ Timing is Interlaced Video, ╠ Stereo Video is not Support, ╚ Digital Separate + Syncs are required.	10011110	158	
		Sixth 18 Byte Data Block:			Detailed Timing
AB	01	╔ Pixel Clock	01100110	102	Descriptor - 1280x720
AC	1D	╚ is 74.250 MHz.	00100001	33	@60Hz Non-Interlaced
AD	00	╔ Horizontal Addressable Video	00000000	0	(720p DTV Timing)
AE	72	╢ is 1280 pixels. Horizontal	01110010	114	(CEA Format #4)
AF	51	╚ Blanking is 370 pixels.	01010001	81	(per CEA861 Standard)
B0	D0	╔ Vertical Addressable Video is	11010000	208	
B1	1E	╢ 720 lines. Vertical Blanking	00011110	30	
B2	20	╚ is 30 lines.	00100000	32	
B3	6E	╔ Horizontal Front Porch is 110 pixels.	01101110	110	
B4	28	╢ Horizontal Sync Pulse Width is 40 pixels	00101000	40	
B5	55	╢ Vertical Front Porch is 5 lines.	01010101	85	
B6	00	╚ Vertical Sync Pulse Width is 5 lines.	00000000	0	
B7	0F	╔ Horizontal Addressable Image Size	11001101	205	
B8	48	╢ is 1039 mm. Vertical Addressable	10110011	179	
B9	42	╚ Image Size is 584 mm.	01000010	66	
BA	00	═ Horizontal Border Size is 0 pixels.	00000000	0	
BB	00	═ Vertical Border Size is 0 lines.	00000000	0	

Address /Offset	Value HEX	Function Description	Value BIN	Value DEC	Notes
BC	1E	╔ Timing is Non-Interlaced Video, ╬ Stereo Video is not Support, ╚ Digital Separate + Syncs are required.	00011110	30	
		Seventh 18 Byte Data Block:			Detailed Timing
BD	8C	╥ Pixel Clock	10001100	140	Descriptor – 720x480
BE	0A	╨ is 27.000 MHz.	00001010	10	@60Hz Non-Interlaced
BF	D0	╥ Horizontal Addressable Video	11010000	208	(480p DTV Timing)
C0	8A	╢ is 720 pixels. Horizontal	10001010	138	(CEA Format #3)
C1	20	╨ Blanking is 138 pixels.	00100000	32	(per CEA861 Standard)
C2	E0	╥ Vertical Addressable Video is	11100000	224	
C3	2D	╢ 480 lines. Vertical Blanking	00101101	45	
C4	10	╨ is 45 lines.	00010000	16	
C5	10	╥ Horizontal Front Porch is 16 pixels.	00010000	16	
C6	3E	╢ Horizontal Sync Pulse Width is 62 pixels	00111110	62	
C7	96	╢ Vertical Front Porch is 9 lines.	10010110	150	
C8	00	╨ Vertical Sync Pulse Width is 6 lines.	00000000	0	
C9	B9	╥ Horizontal Addressable Image Size	10111001	185	
CA	88	╢ is 1039 mm. Vertical Addressable	10001000	136	
CB	21	╨ Image Size is 584 mm.	00100001	33	
CC	00	═ Horizontal Border Size is 0 pixels.	00000000	0	
CD	00	═ Vertical Border Size is 0 lines.	00000000	0	
CE	18	╔ Timing is Interlaced Video, ╬ Stereo Video is not Support, ╚ Digital Separate □ Syncs are required.	00011000	24	
		Eighth 18 Byte Data Block:			Detailed Timing
CF	8E	╥ Pixel Clock	10001110	142	Descriptor – 720x480
D0	0A	╨ is 27.027 MHz.	00001010	10	@60Hz Interlaced
D1	A0	╥ Horizontal Addressable Video	10100000	160	(480i DTV Timing)
D2	14	╢ is 1440 pixels. Horizontal	00010100	20	(CEA Format #7)
D3	51	╨ Blanking is 276 pixels.	01010001	81	(per CEA861 Standard)
D4	F0	╥ Vertical Addressable Video is	11110000	240	
D5	16	╢ 240 lines. Vertical Blanking	00010110	22	
D6	00	╨ is 23 lines.	00000000	0	
D7	26	╥ Horizontal Front Porch is 38 pixels.	00100110	38	
D8	7C	╢ Horizontal Sync Pulse Width is 124 pix.	01111100	124	
D9	43	╢ Vertical Front Porch is 4 lines.	01000011	67	
DA	00	╨ Vertical Sync Pulse Width is 3 lines.	00000000	0	
DB	B9	╥ Horizontal Addressable Image Size	10111001	185	
DC	88	╢ is 1039 mm. Vertical Addressable	10001000	136	
DD	21	╨ Image Size is 584 mm.	00100001	33	
DE	00	═ Horizontal Border Size is 0 pixels.	00000000	0	
DF	00	═ Vertical Border Size is 0 lines.	00000000	0	
E0	98	╔ Timing is Interlaced Video, ╬ Stereo Video is not Support, ╚ Digital Separate □ Syncs are required.	10011000	152	

Address /Offset	Value HEX	Function Description	Value BIN	Value DEC	Notes
E1	00	= No Data	00000000	0	
E2	00	= No Data	00000000	0	
E3	00	= No Data	00000000	0	
E4	00	= No Data	00000000	0	
E5	00	= No Data	00000000	0	
E6	00	= No Data	00000000	0	
E7	00	= No Data	00000000	0	
E8	00	= No Data	00000000	0	
E9	00	= No Data	00000000	0	
EA	00	= No Data	00000000	0	
EB	00	= No Data	00000000	0	
EC	00	= No Data	00000000	0	
ED	00	= No Data	00000000	0	
EE	00	= No Data	00000000	0	
EF	00	= No Data	00000000	0	
F0	00	= No Data	00000000	0	
F1	00	= No Data	00000000	0	
F2	00	= No Data	00000000	0	
F3	00	= No Data	00000000	0	
F4	00	= No Data	00000000	0	
F5	00	= No Data	00000000	0	
F6	00	= No Data	00000000	0	
F7	00	= No Data	00000000	0	
F8	00	= No Data	00000000	0	
F9	00	= No Data	00000000	0	
FA	00	= No Data	00000000	0	
FB	00	= No Data	00000000	0	
FC	00	= No Data	00000000	0	
FD	00	= No Data	00000000	0	
FE	00	= No Data	00000000	0	
FF	5A	= Checksum	01011010	90	

End of example 3

7. APPENDIX B – GTF & CVT Compatibility Issues

The following table list some issues related to the forward and backward compatibility of GTF and CVT generated standard timings in hosts (sources).

	EDID 1.0 & 1.1 Display Device	**EDID 1.2 & 1.3 Display Device**	**EDID 1.4 Display Device**
Host supports EDID data structure definitions up to 1.3 Host supports GTF but does not support CVT.	GTF & CVT were not standards --- no support in EDID 1.0 & 1.1. ---------- Standard timings are derived only from the VESA and Industry Standards and Guidelines for Computer Display Monitor Timing (DMT) Document.	EDID 1.2 & 1.3 provides support for GTF. CVT was not a VESA standard. ---------- If the desired standard timing is a DMT, then use the DMT definition, otherwise use GTF to define the timing parameters.	EDID 1.4 provides support for both GTF & CVT. ---------- If the desired standard timing is a DMT, then use the DMT definition, otherwise use GTF to define the timing parameters.
Host supports EDID data structure definitions up to 1.4 Host supports both CVT & GTF.	GTF & CVT were not VESA standards --- no support in EDID 1.0 & 1.1. ---------- Standard timings are derived using only the VESA and Industry Standards and Guidelines for Computer Display Monitor Timing (DMT) Document	EDID 1.2 & 1.3 provides support for GTF. CVT was not a VESA standard. ---------- If the desired standard timing is a DMT, then use the DMT definition, otherwise use GTF to define the timing parameters.	EDID 1.4 provides support for both GTF & CVT. ---------- If the desired standard timing is a DMT, then use the DMT definition, otherwise use CVT to define the timing parameters.

Notes:

1.) The following requirements are for the source (host) device:

1.1) For a 1.4 compliant source, if Byte 10 (Table 3.26) in the display range limit descriptor is set to a value of "00h" (default GTF support) or "02h" (GTF Secondary Curve support), then any format indicated in the standard timing section (Section 3.9) that does not have a matching DMT shall be derived using the GTF formula.

1.2) For a 1.4 complaint source, if Byte 10 (Table 3.26) in the display range limit descriptor is set to a value of "04h" (CVT support), then any format listed in the standard timing section that does not have a matching DMT shall be derived using the CVT formula with normal blanking, non-interlaced & no-borders.

1.3) For a 1.4 complaint source, if a display range limit descriptor is not listed in EDID, then any format listed in the standard timing section that does not have a matching DMT shall be derived using the CVT formula with normal blanking, non-interlaced & no-borders.

1.4) For a legacy source (supports EDID 1.3 or 1.2), if a display range limit descriptor is or is not listed in EDID, any format listed in the standard timing section that does not have a matching DMT would be driven using the GTF formula.

2.) The following requirements are for the sink device (display):

2.1) Legacy sink devices (supports EDID 1.3 or 1.2) shall support GTF generated timing modes for formats listed in the standard timing section that do not have matching DMTs.

2.2) To ensure compatibility with all sources, new sink devices (supports EDID 1.4) shall support both GTF and CVT variant of the timing reported in the standard timing section for formats that do not have a matching DMTs

3.) A source (host) may support EDID data structure definitions up to version 1.4 (or 1.3) and may not support CVT (or GTF). In this case, the source shall ignore any standard timing (based on the CVT or GTF formula) not listed as a DMT and the source shall not include these video timing formats in the host's list of available formats.
4.) Priority Rule: "CVT has priority over GTF." Exception to this rule: If the use of CVT will result in a forward or backward compatibility issue, then use GTF.
5.) There is a difference between a source that supports CVT (or GTF) and a source that is CVT (or GTF) compliant. Some sources may not be CVT (or GTF) compliant (per the VESA CVT or GTF Standards). This type of host may not be able to generate all CVT (or GTF) video timing formats that are within the display range limits. However, some of these sources may be able to generate a limited number of standard timings using the CVT (or GTF) formula.

8. APPENDIX C - Glossary

Ref. #	Term	Definition
C-1	Active Video Region	The *Active Video Region* is that portion of a transmitted video signal which contains the active video information that is displayed on a monitor's screen. This information is usually generated by a video source (host). In some cases, the displayed video may be generated in the monitor (closed captioning, on screen displays, etc.).
C-2	ASCII	Acronym for the ***A**merican **S**tandard **C**ode for **I**nformation **I**nterchange*. Pronounced *ask-ee*, ASCII is a code for representing English characters as numbers, with each letter assigned a number from 0 to 127. For example, the ASCII code for uppercase *M* is 77. Most computers use ASCII codes to represent text, which makes it possible to transfer data from one computer to another. Text files stored in ASCII format are sometimes called ASCII files. Text editors and word processors are usually capable of storing data in ASCII format, although ASCII format is not always the default storage format. Most data files, particularly if they contain numeric data, are not stored in ASCII format. Executable programs are never stored in ASCII format. The standard ASCII character set uses just 7 bits for each character. There are several larger character sets that use 8 bits, which gives them 128 additional characters. The extra characters are used to represent non-English characters, graphics symbols, and mathematical symbols. Several companies and organizations have proposed extensions for these 128 characters. The DOS operating system uses a superset of ASCII called *extended ASCII* or *high ASCII.* A more universal standard is the ISO Latin 1 set of characters, which is used by many operating systems, as well as Web browsers.
C-3	BCD	Acronym for ***b**inary-**c**oded **d**ecimal,* a format for representing decimal numbers (integers) in which each digit is represented by four bits (a *nibble*). For example, the number 375 would be represented as: 0011 0111 0101 One advantage of BCD over binary representations is that there is no limit to the size of a number. To add another digit, you just need to add a new 4-bit sequence. In contrast, numbers represented in binary format are generally limited to the largest number that can be represented by 8, 16, 32 or 64 bits.
C-4	BIOS	(bī´ōs) Acronym for ***b**asic **i**nput/**o**utput **s**ystem*, the built-in software that determines what a computer can do without accessing programs from a disk. On PCs, the BIOS contains all the code required to control the keyboard, display screen, disk drives, serial communications, and a number of miscellaneous functions. The BIOS is typically placed in a ROM chip that comes with the computer (it is often called a *ROM BIOS*). This ensures that the BIOS will always be available and will not be damaged by disk failures. It also makes it possible for a computer to boot itself. Because RAM is faster than ROM, though, many computer manufacturers design systems so that the BIOS is copied from ROM to RAM each time the computer is booted. This is known as *shadowing*. Many modern PCs have a *flash BIOS,* which means that the BIOS has been recorded on a flash memory chip, which can be updated if necessary.

Ref. #	Term	Definition
C-5	CEA	Acronym for ***C**onsumer **E**lectronics **A**ssociation.* CEA has developed standards and specifications for the Consumer Electronics Industry. More information is available at www.ce.org .
C-6	CIE	Acronym for ***C**ommission **I**nternationale de l'**E**clairage.* CIE is a technical, scientific and cultural, non-profit autonomous organization devoted to international cooperation and exchange of information among its member countries on all matters relating to the science and art of lighting. Founded in the early 1900s, CIE has developed several Chromaticity Diagrams (1931 - 2°, 1976 – UCS, etc.). More information is available at www.cie.co.at .
C-7	CVT	Shorthand method of referring to VESA's ***C**oordinated **V**ideo **T**iming* Standard. CVT is a method for generating a consistent and coordinated set of standard formats, display refresh rates, and timing specifications for computer display products. More information is available at www.vesa.org .
C-8	DCM	Shorthand method of referring to VESA's ***D**isplay **C**olor **M**anagement* Standard. The DCM Standard defines the overall requirements, data collection, data conversion and data storage for monitor-specific data needed to perform display color management as part of a color managed computer system. More information is available at www.vesa.org .
C-9	DDC	Acronym for ***D**isplay **D**ata **C**hannel,* a VESA standard for a serial communications link (based on I^2C protocols) between a monitor and a video adapter. Using DDC, a monitor can inform the video card about its properties, such as maximum resolution, color depth and supported video timing modes. The video card can then use this information to ensure that the user is presented with valid options for configuring the display. The VESA DDC standard is obsolete and has been superseded by the VESA E-DDC Standard. DDC can also refer to an addressing method which allows the host (source) to read up to 256 bytes of EDID data. More information is available at www.vesa.org .
C-10	DI-EXT	Shorthand method of referring to VESA's ***D**isplay **I**nformation **Ext**ension* Block Standard. DI-EXT is an extension block to the base (block 0) EDID. DI-EXT contains additional information related to the digital interface and display feature set that is not available in the base (block 0) EDID. More information is available at www.vesa.org .
C-11	DMT	Shorthand method of referring to the "VESA and Industry Standards and Guidelines for Computer ***D**isplay **M**onitor **T**iming* (DMT) Standard". The DMT standard lists the timing parameters for VESA and industry video timing formats. More information is available at www.vesa.org .
C-12	DPVL-EXT	Shorthand method of referring to VESA's ***D**igital **P**acket **V**ideo **L**ink **Ext**ension* Block. DPVL-EXT is defined in the VESA Digital Packet Video Link (DPVL) Standard. The DPVL Standard defines video packet structures, a capability management scheme and a monitor control scheme. DPVL-EXT is an extension block to the base (block 0) EDID. More information is available at www.vesa.org .
C-13	DTV	Acronym for ***D**igital **T**elev**i**sion.*
C-14	DVI	Acronym for ***D**igital **V**isual **I**nterface.* DVI is a digital video interface (using TMDS protocols) specification that was defined by the Digital Display Working Group (DDWG). More information is available at www.ddwg.org .

Ref. #	Term	Definition
C-15	E-DDC	Acronym for ***E**nhanced-**D**isplay **D**ata **C**hannel,* a VESA standard for a serial communications link (based on I^2C protocols) between a monitor and a video adapter. Using E-DDC, a monitor can inform the video card about its properties, such as maximum resolution, color depth and supported video timing modes. The video card can then use this information to ensure that the user is presented with valid options for configuring the display. E-DDC can also refer to an addressing method which allows the host (source) to read up to 32 Kbytes of EDID data. More information is available at www.vesa.org .
C-16	EDID	Acronym for ***E**xtended **D**isplay **I**dentification **D**ata.* EDID can refer to a VESA standard data format that contains basic information about a monitor and its capabilities, including vendor information, maximum image size, color characteristics, factory pre-set timings, frequency range limits, and character strings for the monitor name and serial number. The information is stored in the display and is used to communicate with the system through a Display Data Channel (DDC), which sits between the monitor and the PC graphics adapter. The system uses this information for configuration purposes, so the monitor and system can work together. The term 'EDID' may refer to configuration data that is stored in a display and can be read/decoded by a host. EDID may refer to base EDID (Block 0) or a base EDID (Block 0) plus one or more extension blocks. The term EDID may also refer to a process for storing and reading the data. The VESA EDID standard is obsolete and has been superseded by the VESA E-EDID Standard. More information is available at www.vesa.org .
C-17	E-EDID	Acronym for ***E**nhanced **E**xtended **D**isplay **I**dentification **D**ata.* The term E-EDID may refer to a process for storing and reading the data. In addition, the term E-EDID is shorthand for the VESA Enhanced Extended Display Identification Data Standard. More information is available at www.vesa.org .
C-18	EIA	Abbreviation for ***E**lectronic **I**ndustries **A**lliance. EIA* is a trade association representing the U.S. high technology community. It began in 1924 as the Radio Manufacturers Association. The EIA sponsors a number of activities on behalf of its members, including conferences and trade shows. In addition, it has been responsible for developing some important standards, such as the RS-232, RS-422 and RS-423 standards for connecting serial devices.
C-19	EISA ID	Acronym for ***E**xtended **I**ndustry **S**tandard **A**rchitecture **I**dentification **D**ata*. The EISA ID code is used to represent an ID manufacturer name. It is a 2-byte representation of the monitor's manufacturer 3 letter code using compressed ASCII, "00001=A" ... "11010=Z". EISA manufacturer IDs are issued by Microsoft. Contact by email or fax: E-mail: pnpid@microsoft.com Fax: 425-936-7329, Attention PNPID in Building 27. URL: Refer to www.microsoft.com/whdc/hwdev/pnpid.mspx for more information on EISA ID.
C-20	FPD	Acronym for ***F**lat **P**anel **D**isplay.*
C-21	Frame Lock	As applied to electronic displays, Frame Lock is achieved when there is a constant time relationship between elements of the image at the display's input (the external interface) and the visible appearance of the corresponding elements in the displayed image.

Ref. #	Term	Definition
C-22	Gamma	The term *Gamma* is used to signify the exponent of a power function describing the transfer characteristics of a *Display* when such a curve is an accurate (or adequate) description. Commonly used as a short-hand term meaning the *Display Transfer Characteristic* of any *Display*.
C-23	GTF	Shorthand method of referring to VESA's ***G****eneralized* ***T****iming* ***F****ormula* Standard. GTF is a standard method of creating video timing modes. More information is available at www.vesa.org .
C-24	HA	HA refers to ***H****orizontal* ***A****ctive* pixels. HA is part of a complete video timing format definition. HA defines the number of active pixels on a horizontal line that can be displayed on a monitor screen. For more information, refer to section 3.12.
C-25	HB	HB refers to ***H****orizontal* ***B****order*. HB is part of a complete video timing format definition. HB defines the number of pixels on a horizontal line that is located between the HA and HBL regions. HB can be in two locations --- before and after HA. Portions of the HB may be displayed on a monitor screen. For more information, refer to section 3.12.
C-26	HBL	HBL refers to ***H****orizontal* ***B****lanking*. HBL is part of a complete video timing format definition. HBL defines the number of pixels on a horizontal line where HA and HB are not present. Portions of the HBL may be displayed on a monitor screen. For more information, refer to section 3.12.
C-27	HDMI	Shorthand method of referring to the ***H****igh-****D****efinition* ***M****ultimedia* ***I****nterface* Specification. HDMI is a digital video and audio interface (using TMDS protocols) specification that is commonly being used in consumer electronic devices (sources and displays). Refer to www.hdmi.org for more information on HDMI.
C-28	HSO	HSO refers to ***H****orizontal* ***S****ync* ***O****ffset*. HSO is part of a complete video timing format definition. HSO defines the number of pixels on a horizontal line which are located between the end (trailing edge) of HA and the beginning (leading edge) of the horizontal sync pulse. HSO includes the HB and the horizontal front porch regions. For more information, refer to section 3.12.
C-29	HSPW	HSPW refers to ***H****orizontal* ***S****ync* ***P****ulse* ***W****idth*. HSPW is part of a complete video timing format definition. HSPW defines the number of pixels on a horizontal line which are located between the leading and trailing edges of the horizontal sync pulse. For more information, refer to section 3.12.
C-30	IEC	Acronym for ***I****nternational* ***E****lectrotechnical* ***C****ommission.* IEC is the authoritative worldwide body responsible for developing consensus global standards in the electrotechnical field. Refer to http://www.iec.ch/index.html for more information on IEC.
C-31	ISO	Acronym for ***I****nternational* ***O****rganization for* ***S****tandardization*. ISO is the world's largest developer of standards (both technical and non-technical). Refer to http://www.iso.org/iso/en/ISOOnline.frontpage for more information on ISO.
C-32	Letterbox	A coded frame having horizontal bars, usually black, present at the top and bottom.
C-33	LSB	Acronym for ***L****east* ***S****ignificant* ***B****yte.* It means if 2 or more bytes of data are stored in a system, the data is stored least significant byte first. For example, a certain Product ID may be '7203(hex)'. In the base EDID (block 0), the 2 byte Product ID code is stored as '03h' at address **0Ah** and '72h' at address **0Bh** or least significant byte is listed first. The most significant byte is listed last.
C-34	LS-EXT	Shorthand method of referring to VESA's ***L****ocalized* ***S****tring* ***Ext****ension* Block. LS-EXT is defined in the VESA Enhanced EDID Localized String Extension (LS-EXT) Standard. LS-EXT is an extension block to the base (block 0) EDID. More information is available at www.vesa.org .

Ref. #	Term	Definition
C-35	Native Pixel Format	Native Pixel Format is defined as the number of physical pixels along the horizontal axis by the number of physical pixels along the vertical axis of the display device. Note that some display technology implementations do not have an array of "physical pixels" but instead can be considered to have an array of virtual or logical pixels. In these cases, the Native Pixel Format is defined as the number of virtual or logical pixels along the horizontal axis by the number of virtual or logical pixels along the vertical axis of the display device that the display manufacturer has determined provides an optimum image.
C-36	Off	Off is one of 4 monitor power states defined in the VESA Display Power Management Signaling (DPMS) Standard. Off is also one of 2 monitor power states defined in the VESA Display Power Management (DPM) Standard. The Off state provides for the maximum amount of power savings. The amount of power savings (in watts) in the Off state is monitor design dependant. The amount of recovery time is also system design dependant. In some monitor designs, recovery from the Off state may require user intervention. Note that the VESA DPM Standard has superseded (replaced) the VESA DPMS Standard. More information is available at www.vesa.org.
C-37	On	On is one of 4 monitor power states defined in the VESA Display Power Management Signaling (DPMS) Standard. On is also one of 2 monitor power states defined in the VESA Display Power Management (DPM) Standard. On refers to the state of the display when it is in full operation. The On state provides for no power savings. Note that the VESA DPM Standard has superseded (replaced) the VESA DPMS Standard. More information is available at www.vesa.org.
C-38	Pillarbox	A coded frame having vertical bars, usually black, present at the left and right edge.
C-39	PTB	Shorthand method of referring to VESA's ***P**referred **T**iming **B**it*. EDID data structure version 1, revision 3 requires the EDID Preferred Timing Bit (PTB) to be set to one. EDID data structure version 1, revision 4 changed the PTB definition to the following: 'Preferred Timing Mode includes (if PTB = '1') or does not include (if PTB = '0') the native pixel format and preferred refresh rate of the display device.' The PTB is located at bit 1 of the "Feature Support Byte" (at address **18h**). Refer to section 3.6.4.
C-40	PTM	Shorthand method of referring to VESA's ***P**referred **T**iming **M**ode*. EDID data structures version 1, revision 3 and version 1, revision 4 requires the preferred timing mode be stored in the first 18 Byte Data Block. The display manufacturer defines the "Preferred Timing Mode (PTM)" as the video timing mode that will produce the best quality image on the display's viewing screen. For most flat panel displays (FPD), the preferred timing mode will be the panel's "native timing" and "native resolution".
C-41	Standby	Standby is one of 4 monitor power states defined in the VESA Display Power Management Signaling (DPMS) Standard. Standby (now Off) is also one of 2 monitor power states defined in the VESA Display Power Management (DPM) Standard. The Standby state provides for a minimal amount of power savings --- somewhere between zero power savings in the On state and substantial power savings in the Suspend State. The amount of power savings (in watts) in the Standby state is monitor design dependant. The amount of recovery time is defined as short --- also system design dependant. In the VESA DPM Standard, the Standby state has been translated to the Off state. Note that the VESA DPM Standard has superseded (replaced) the VESA DPMS Standard. More information is available at www.vesa.org.

Ref. #	Term	Definition
C-42	Suspend	Suspend is one of 4 monitor power states defined in the VESA Display Power Management Signaling (DPMS) Standard. Suspend (now Off) is also one of 2 monitor power states defined in the VESA Display Power Management (DPM) Standard. The Suspend state provides for a substantial amount of power savings --- somewhere between minimal power savings in the Standby state and maximum power savings in the Off State. The amount of power savings (in watts) in the Suspend state is monitor design dependant. The amount of recovery time is defined as longer than the Standby recovery time --- also system design dependant. In the VESA DPM Standard, the Suspend state has been translated to the Off state. Note that the VESA DPM Standard has superseded (replaced) the VESA DPMS Standard. More information is available at www.vesa.org.
C-43	VA	VA refers to ***V**ertical **A**ctive* lines. VA is part of a complete video timing format definition. VA defines the number of horizontal lines in a vertical field that can be displayed on a monitor screen. For more information, refer to section 3.12.
C-44	VB	VB refers to ***V**ertical **B**order*. VB is part of a complete video timing format definition. VB defines the number of horizontal lines in a vertical field that is located between the VA and VBL regions. VB can be in two locations --- before and after VA. Portions of the VB may be displayed on a monitor screen. For more information, refer to section 3.12.
C-45	VBE	Shorthand method of referring to ***VESA BIOS E**xtension* Standards. VBE refers to a group of VESA Standards: VBE/Accelerator Functions; VBE/Audio Interface; VBE/Core Functions; VBE/Display Data Channel; VBE Power Management & VBE/Serial Control Interface. More information is available at www.vesa.org .
C-46	VBL	VBL refers to ***V**ertical **B**lanking*. VBL is part of a complete video timing format definition. VBL defines the number of lines on a vertical field where VA and VB are not present. Portions of the VBL may be displayed on a monitor screen. For more information, refer to section 3.12.
C-47	VIAD	Shorthand method of referring to VESA's ***V**ideo **I**mage **A**rea **D**efinition* Standard. VIAD is a standard method of defining the usable image area for CRT displays. More information is available at www.vesa.org .
C-48	VSO	VSO refers to ***V**ertical **S**ync **O**ffset*. VSO is part of a complete video timing format definition. VSO defines the number of horizontal lines in a vertical field which are located between the end (trailing edge) of VA and the beginning (leading edge) of the vertical sync pulse. VSO includes the VB and the vertical front porch regions. For more information, refer to section 3.12.
C-49	VSPW	VSPW refers to ***V**ertical **S**ync **P**ulse **W**idth*. VSPW is part of a complete video timing format definition. VSPW defines the number of horizontal lines in a vertical field which are located between the leading and trailing edges of the vertical sync pulse. For more information, refer to section 3.12.
C-50	VTB-EXT	Shorthand method of referring to VESA's ***V**ideo **T**iming **B**lock **Ext**ension* Data Standard. VTB-EXT is an extension block to the base (block 0) EDID. VTB-EXT allows for the storage of additional video timing information that may not fit in the base (block 0) EDID. More information is available at www.vesa.org .

9. APPENDIX D - Answers To Commonly Asked Questions

Ref. #	Question	Answer
D-1	What is relationship between EDID Data Structures Version 1 Revision 0, Version 1 Revision 1, Version 2 Revision 0, Version 1 Revision 2, Version 1 Revision 3 and Version 1 Revision 4 defined in the DDC, EDID and E-EDID Standards?	Below is the history of EDID Data Structure Definitions: 1. EDID data structure 1.0 was the original 128-byte data format introduced in the DDC Standard Version 1.0 Revision 0 (August 12, 1994). 2. EDID data structure 1.1 was introduced in the EDID Standard Version 2 Revision 0 (April 1996). Structure 1.1 added definitions for monitor descriptors as an alternate use of the space originally reserved for detailed timings, as well as definitions for previously unused fields. 3. EDID data structure 1.2 was introduced in EDID Standard Version 3 (November 13, 1997). Structure 1.2 added definitions to existing data fields. EDID data structure 2.0 (a 256 byte definition) was also defined in the Version 3 standard. 4. EDID data structure 1.3 was defined in the E-EDID Standard Release A (September 2, 1999). The 1.3 data structure added definitions for secondary GTF curve coefficients. EDID 1.3 was based on the same core as all other EDID 1.x structures. Structure 1.3 is a superset of structure 1.2. The main difference between the two is that 1.3 allows the Monitor Range Limits descriptor to define coefficients for a secondary GTF curve, and mandates a certain set of monitor descriptors. 5. The current E-EDID Standard Release A Revision 1 (Date is TBD) defines the EDID data structure 1.4. The new data structure 1.4 includes support for CVT and some new monitor timing and data descriptors. Each new EDID data structure adds enhancements to the EDID definition and it supersedes the older generation data structure. It should be noted that the EDID data structure 2.0 defined in the EDID Version 3 Standard has not been widely adopted, although the standard is still considered valid. Today, the most commonly used EDID data structure is version 1.3. However, new designs, especially those intended for the standard PC and CE markets, are strongly urged to use only the new data structure 1.4 defined in this document (E-EDID, Release A, Revision 1).
D-2	What should 'ID Manufacturer Name' field contain?	Ref.: Section 3.4.1 (E-EDID Standard Release A, Revision 2) This field should contain the registered ISA (Industry Standard Architecture) -ID (Identification Data) code for the manufacturer' name. Note that ISA was formally known as EISA. ISA codes are now issued by Microsoft as part of their plug and play activity. Contact via e-mail: PnPID@Microsoft.com. Contact via fax: 425-936-7329, Attention PNPID in Building 27. URL: Refer to http://www.microsoft.com/whdc/system/pnppwr/pnp/pnpid.mspx. for more information on ISA ID. **Note:** Previous versions of this standard made reference to BCPR as provider of this information. This is no longer correct. However, existing ISA ID codes issued by BCPR remain valid.
D-3	What should the 'ID Product Code' field contain?	Ref.: Section 3.4.2 (E-EDID Standard Release A, Revision 2) A display manufacturer assigned identifier (2 bytes --- LSB) for the product type, e.g. the model number. Note that some host SW expects the combination of the 'manufacturer code' + the 'ID product code' to give a unique identifier.

Ref. #	Question	Answer
D-4	Table 3.22 Decode for Stereo Modes If bits 5 & 6 = 0 what should bit 0 equal?	Ref.: Table 3.22 (E-EDID Standard Release A, Revision 2) Bit 0 is defined as a "don't care" (i.e., it should be ignored) in this case. When both bits 5 & 6 are set to zero, the display is indicating that it has no support for stereo operation.
D-5	In section 3.10.2 Detailed Timing Description: Is the following true? Horizontal sync offset = Horizontal front porch, if Horizontal border = 0.	Ref.: Section 3.10.2 (E-EDID Standard Release A, Revision 1) Yes
D-6	Does 'Horizontal Addressable Video in pixels' = the total number of pixels on a horizontal line?	Ref.: Sections 3.10.2 (E-EDID Standard Release A, Revision 2) No; one complete horizontal line consists of both the Horizontal Addressable Video, Horizontal Border and Horizontal Blanking periods. Therefore, the total number of pixels in one full horizontal line time is obtained by summing these values (as provided by the third through fifth bytes of a Detailed Timing Description; see Table 3.21)
D-7	Is 'Image aspect ratio' = (Horizontal addressable pixel) ÷ (Vertical addressable pixel)?	Ref.: Section 3.9 (E-EDID Standard Release A, Revision 2) Yes, assuming that the pixels are "square." All VESA timing standards assume "square" pixels; this may not be the case for timings from other sources, and so the Standard Timing codes should be used only for timings which conform to the VESA CVT, DMT, GTF, etc., standards.
D-8	If calculated aspect ratio is not 16 : 10 AR, 4 : 3 AR, 5 : 4 AR or 16 : 9 AR what timing description should be used?	Ref.: Section 3.9 (E-EDID Standard Release A, Revision 2) The Standard Timings Identification code may not be used to identify timings which do not match one of these standard aspect ratios. Support for such timings must be indicated elsewhere, e.g., by use of a Detailed Timing Descriptor.
D-9	How should VESA standard timings not listed in the 'established timings' section be handled?	Ref.: Section 3.9 (E-EDID Standard Release A, Revision 2) The 'standard timing identification' fields (2 bytes each) provide for a coded way to identify timings not included in the 'established timings' section. It is also possible to fully describe a required timing in a 'detailed timing descriptor'.
D-10	If I want to use the 'standard timing identification' fields, where do I get the 'Horizontal addressable pixel' and 'image aspect ratio' for a particular timing?	Ref.: Section 3.9 (E-EDID Standard Release A, Revision 2) VESA timing standards (VESA and Industry Standards and Guidelines for Computer Display Monitor Timing (DMT), Version 1.0, Revision 10; October 29, 2004) include these parameters.
D-11	If I want to use a 'detailed timing descriptor' block, where do I get the detailed information?	Ref.: Section 3.10.2 (E-EDID Standard Release A, Revision 2) If it is a standard VESA timing, then all details are part of the VESA and Industry Standards and Guidelines for Computer Display Monitor Timing (DMT), Version 1.0, Revision 10, October 29, 2004. If it is a proprietary timing, then details need to be established by the developer.
D-12	Section 3.8 Established Timing Section says "...a list of one-bit flags, which may be used to indicate support for established VESA and other common timings in a very compact form ..." Does 'support' mean that the mode is pre-set in the monitor or that monitor is capable of handling the mode?	Ref.: Section 3.8 (E-EDID Standard Release A, Revision 2) It is the intention of the VESA specification that all modes selected here are monitor supported modes and should not need image size and center adjustments by the end user. Different manufacturers have applied different interpretations, it appears that some define 'support' to mean that the monitor is capable of handling the mode but may require user adjustment of image size, centering, etc.

Ref. #	Question	Answer
D-13	In Table 3.30 – Additional Color Point Descriptor Definition - A Value of '00h' at Byte 10 indicates 'No color point data follows' Does this mean that only white gamma follows or neither white chromaticity nor gamma follow?	In Table 3.30 (E-EDID Standard Release A, Revision 2), an index value = 00h means that neither white point chromaticity nor white gamma values follow.
D-14	In Table 3.30: What binary index value should the white point index start from? Is it arbitrary?	Ref.: Table 3.30 (E-EDID Standard Release A, Revision 2) It is arbitrary and left to individual manufacturers. However, there is white color and gamma data stored in bytes 24 - 27 (decimal) with no explicit index number. Implementers may wish to assume that this is an implicit index number of 1 and hence the explicit index numbers in a descriptor block should start at 2.
D-15	In section 3.10.3.5: How many color point monitor descriptors are allowed? One or up to four?	Ref.: Section 3.10.3.5 (E-EDID Standard Release A, Revision 2) For EDID data structure version 1.4, up to six color points may be defined in 3 monitor descriptor blocks. This assumes that the monitor range limits and monitor name are not used.
D-16	What is the most reliable way for a graphics sub-system to determine the operating range of the attached monitor?	Ref.: Section 3.10.3.3 (E-EDID Standard Release A, Revision 2) For EDID data structure version 1.4, it is recommended that the Display Range Limit Descriptor (if provided) be used. Monitor operating range limits cannot be reliably inferred from any other source within the EDID.
D-17	Which EDID data structure should I use with a DVI implementation?	The DVI specification (version 1.0) permits the use of EDID data structures 1.2 and 2.0 for interim designs but indicates that they want to move to EDID data structure 1.3. However, VESA recommends that you use EDID data structure version 1.4 which is defined in this document.
D-18	Are there any dependencies on EDID for implementation of DVI hot-plugging?	No, the hot-plugging scheme described in the DVI specification is independent of the EDID content.
D-19	In EDID, how do you count the week value? Do you start counting on the first Monday or the first Sunday of the new year?	Ref.: Section 3.4.4 (E-EDID Standard Release A, Revision 2) How one defines the week of manufacture is up to the individual display manufacturer. However, one way is to count January 1-7 as week 1, January 8-15 as week 2 and so on. This will give consistent results, regardless of the year, and will always yield a value of 54 or less. You can also count based on the week number (Sunday-Saturday).
D-20	Has a common address been set for the EDID memory in the DFP, P&D and DVI standards? In the past A0h was the only address, until P&D introduced A2h.	The Enhanced EDID and Enhanced DDC standards refer only to A0h and 60h. This is the address used by DFP, DVI and HDMI. Since P&D was not widely adopted, it is anticipated that support for P&D will fade and the use of A2h will diminish.
D-21	For monitors using DVI connectors, how do you set the Video Input Definition byte? Doesn't the digital port share the same EDID with the analog one on a DVI-1 connector?	Ref: Section 3.6.1 (E-EDID Standard Release A, Revision 2) The DVI-I connector includes one analog input and one digital input. Only one port (analog or digital) can be active. You must have 2 EDID tables (one analog and one digital) stored in the monitor. If the analog input is active, then the DDC channel transmits the analog EDID table and bit 7 of the byte at address **14h** (Video Input Definition) is set to zero. If the digital input is active, then the DDC channel transmits the digital EDID table and bit 7 of the byte at address **14h** (Video Input Definition) is set to one. An alternative to using DVI-I is to use VESA's M-1 connector or 2 separate (one VGA and one DVI-D) connectors.

Ref. #	Question	Answer
D-22	I have a question regarding the 18 Byte Descriptors (Detailed Timing) Section of the E-EDID Standard (sec. 3.10, pg. 30). Our display supports one resolution — 1024x768@60Hz. Are we required to fill in the remaining three descriptor blocks with valid data? I see we are required to give a display range limits descriptor and a display product name descriptor, as well as another descriptor. Is it OK to fill these with 'junk' or random data?	Ref: Section 3.10 (E-EDID Standard Release A, Revision 2) All four 18 Byte Descriptors must contain data. 'Junk' or 'random data' cannot be used. The first 18 Byte Descriptors must contain the Preferred Timing Mode --- in this case, 1024x768@60Hz. For EDID data structure version 1, revision 3, the use of the Display Range Limit Descriptor and the Display Product Name Descriptor are required. For EDID data structure version 1, revision 4, the use of the Display Range Limit Descriptor and the Display Product Name Descriptor are optional (but recommended). If the Display Range Limit Descriptor is used for a single mode (frequency) monitor, define the horizontal and vertical pull in ranges. Any unused 18 Byte Descriptors must be filled with the Dummy Descriptor --- data tag '10h'. Refer to section 3.10.3.11.
D-23	To implement the E-EDID EEPROM Standard, does one also need the E-EDID Standard?	The E-EDID Standard is not necessary, but would be helpful. However, E-DDC is necessary because the EEPROM will need to implement the block pointer (offset pointer at address '60h') described in the E-DDC Standard.
D-24	In the E-EDID Standard (Rel. A, Rev. 2) in section 3.4.4, table 3.8 it states "A value of '00h' indicates that the Week of Manufacture is not specified". Is it also okay to set the value '00h' if the 'year' of manufacture field is not used? Do you have to use the year that you manufactured? It is a bit of trouble to change the manufacture year for the same product every year. Can you use the year of development instead?	Ref: Section 3.4.4 (E-EDID Standard Release A, Revision 2) The week of manufacture field is optional and if not used, enter a value of '00h' at address **10h**. The year of manufacture field is required and shall be set according to the definition in the E-EDID Standard. Monitors manufactured in 2005, for example, would use the value '0Fh'. You have the option to declare the Model Year --- you can do this by entering 'FFh' at address **10h** (Week of Manufacture). The data stored at address **11h** now contains the Model Year.
D-25	In E-EDID (Release A, Revision 2) Table 3.19 states that there is a formula for horizontal active pixel and aspect ratio. Is this VESA DMT, GTF or CVT?	Ref: Section 3.9 (E-EDID Standard Release A, Revision 2) The formula in Table 3.19 just describes the method to encode the data for the standard timing block in EDID. This block has primarily been used to indicate support for standard timings in DMT. The 2-byte codes for this encoding are actually shown in the DMT Standard. If a video timing mode is not listed in DMT, then use the GTF/CVT formulas to generate the timing parameters. An example would be 1024x768@80Hz, which would be encoded with the 2-byte code of '61h' & '54h'. Since there is no VESA standard for this format and refresh rate combination, this 2-byte code would indicate that the monitor supports a GTF or CVT-based timing for this mode. Note: EDID data structure version 1.3 supports GTF. For EDID data structure version 1.4, GTF has been replaced by CVT.
D-26	How do I handle backward compatibility between a host (source) that can decode EDID data structure version 1.3 when connected to a display (sink) that contains EDID data structure version 1.4?	Refer to VESA's "Plug & Play" Standard. A source that can only decode EDID data structure version 1.3 should ignore any EDID 1.4 data fields that it does not understand.
D-27	Is it possible to distinguish the display technology (CRT, LCD, PDP, etc.) being used on a video interface if the DI-EXT extension is not present in the monitor?	Ref: Section 3.10.1 (E-EDID Standard Release A, Revision 2) There is no way to determine the display technology being used from the base EDID (block 0). However, you can look at the preferred timing in the first 18-Byte Data Block (the detailed timing definition) in the base EDID. Most LCDs use a 60Hz rate, while most CRTs use 75Hz or 85Hz. While this is not an absolute method, it does provide some clues.

Ref. #	Question	Answer
D-28	What are Established Timings and why are they different than Standard Timings and Detailed Timings?	Ref: Section 3.8 (E-EDID Standard Release A, Revision 2) Established Timings contain a list of industry and VESA standard timings commonly used in the PC industry. Established Timings include Established Timing I & II and Manufacturer's Timings. Refer to Table 3.18. All video timing modes listed in the Established Timings are defined in the VESA DMT Standard. Note that EDID Data Structure version 1.4 defines an optional Established Timing III as a monitor descriptor. Refer to section 3.10.3.9. Established Timings III lists those display monitor timings (DMTs) that are listed in the VESA and Industry Standards and Guidelines for Computer Display Monitor Timing (DMT) Standard but are not included in Established Timings I or II or Manufacturer's Timings. Because Established Timings are well-known and documented, they can be represented by a single bit set in EDID. Note that Established Timings do not indicate any order of priority for the video timing modes that are listed.
D-29	What are Standard Timings and why are they different than Established Timings and Detailed Timings?	Ref: Section 3.9 (E-EDID Standard Release A, Revision 2) Standard Timings are used to represent VESA standard timings that are listed in the VESA and Industry Standards and Guidelines for Computer Display Monitor Timing (DMT) but are not included in Established Timings I or II or Manufacturer's Timings. A 2-byte formula is used to give minimal information about the format and refresh rate so they can be referenced to a known timing. The 2-byte codes for DMT defined timings are listed in the VESA and Industry Standards and Guidelines for Computer Display Monitor Timing (DMT). For video timing modes that are not listed in the VESA and Industry Standards and Guidelines for Computer Display Monitor Timing (DMT) document, use GTF to generate the 2-byte Standard Timing codes. This allows displays to indicate support for new timing standards without the need to revise the EDID or the DMT Standards when those timings are created. Note that it is not good practice to list (repeat) an Established Timing in the Standard Timings section. This is a redundant listing. Note that the order of listing Standard Timings indicates the order of priority for the video timing modes that are listed.
D-30	What are Detailed Timings and why are they different than Established Timings and Standard Timings?	Ref: Section 3.10.2 (E-EDID Standard Release A, Revision 2) Detailed Timings are stored in the 18 byte Descriptors located at EDID addresses **36h**, **48h**, **5Ah** and **6Ch**. This allows the display to give a complete timing definition. Detailed Timings allow the display to give details of custom timings that cannot be expressed in the Established or Standard Timing sections. Note that it is not good practice to list (repeat) an Established Timing or a Standard Timing in the Detailed Timing section. This is a redundant listing. There is one exception. The Preferred Timing Mode (listed in the First 18 Byte Descriptor) may be repeated in the Established Timing or the Standard Timing sections. The display manufacturer defines the "Preferred Timing Mode (PTM)" as the video timing mode that will produce the best quality image on the display's viewing screen.

Ref. #	Question	Answer
D-31	In what section of the EDID timing code is the maximum resolution of the display set?	When a host (source) interprets the EDID content, all three timings (Established, Standard & Detailed) must be considered to get a complete picture of the formats and timings supported by the display. The maximum resolution of the display would correspond to the maximum format expressed by any of the three timing sections. This is an indication of the maximum resolution supported by the display. However, it is possible that a CVT compliant display may support a higher resolution than is indicated in the base EDID table. In this case, the maximum resolution can not be determined.
D-32	We are about to submit our LCD monitor test results to Microsoft to get their certification. But at this time, while reading the EDID of our LCD, in the monitor type, the word CRT appears instead of LCD. In reading the E-EDID Standard, there is no information to solve this problem. Where do we modify the EDID so the Microsoft software EDIDW2K.exe displays LCD, not CRT?	The base EDID does not indicate the monitor type (CRT, LCD, etc.). The monitor type is indicated (using manual input) in the Microsoft Windows Hardware Quality Labs (WHQL) Test Tool. Run the test tool. In the first screen, you have to manually input the following information; 1. Enter monitor screen size 2. Select monitor type (CRT, LCD, etc) 3. Select connector type (VGA, DVI, etc). Then complete the tests and the correct monitor type will appear in the Test Log Report.
D-33	According to EDID Data Structure 1.3, there are two bytes for ID product code. But if the code is too long, or there are letters in the product code how can I write these two bytes? (example XX-15SX)	It is important not to mix up the meaning of Product ID Code, Product Name and Product Model Number. Product ID is a 2 byte hexadecimal code (defined by monitor manufacturer), which resides at addresses **0Ah** and **0Bh** (least significant byte first) in the base (block 0) EDID. (For example, ViewSonic has a 23" LCD whose Product ID is '7203(hex)'. The code is stored as '03h' at address **0Ah** and '72h' at address **0Bh**. Product Name is the name placed on the bezel of the monitor, on the carton, in the user guide, etc. The ViewSonic monitor above has a Product Name of VP230mb Product Model Number is the model number used by sales, RMA repair, etc. The ViewSonic monitor above has a model number of VLCDS22494-1b. The ID Code (stored in the base EDID) points to data in an INF file. Microsoft defines the information required in the INF file, which contains monitor manufacturer's name, Product Name, Product Model Number, and other pieces of information.

10. APPENDIX E – ASCII Reference Tables

Appendix E includes ASCII Tables. These are for reference only. For more information on ASCII Codes, refer to ISO/IEC 8859-1: 1998 Information Technology - 8-bit single-byte coded graphic character sets - Part 1: Latin alphabet No. 1 - ASCII Codes

Table ASCII -I

Dec	Hex	Char	Dec	Hex	Char	Dec	Hex	Char	Dec	Hex	Char
0	00	Null	32	20	Space	64	40	@	96	60	`
1	01	Start of heading	33	21	!	65	41	A	97	61	a
2	02	Start of text	34	22	"	66	42	B	98	62	b
3	03	End of text	35	23	#	67	43	C	99	63	c
4	04	End of transmit	36	24	$	68	44	D	100	64	d
5	05	Enquiry	37	25	%	69	45	E	101	65	e
6	06	Acknowledge	38	26	&	70	46	F	102	66	f
7	07	Audible bell	39	27	'	71	47	G	103	67	g
8	08	Backspace	40	28	(	72	48	H	104	68	h
9	09	Horizontal tab	41	29	)	73	49	I	105	69	i
10	0A	Line feed	42	2A	*	74	4A	J	106	6A	j
11	0B	Vertical tab	43	2B	+	75	4B	K	107	6B	k
12	0C	Form feed	44	2C	,	76	4C	L	108	6C	l
13	0D	Carriage return	45	2D	-	77	4D	M	109	6D	m
14	0E	Shift out	46	2E	.	78	4E	N	110	6E	n
15	0F	Shift in	47	2F	/	79	4F	O	111	6F	o
16	10	Data link escape	48	30	0	80	50	P	112	70	p
17	11	Device control 1	49	31	1	81	51	Q	113	71	q
18	12	Device control 2	50	32	2	82	52	R	114	72	r
19	13	Device control 3	51	33	3	83	53	S	115	73	s
20	14	Device control 4	52	34	4	84	54	T	116	74	t
21	15	Neg. acknowledge	53	35	5	85	55	U	117	75	u
22	16	Synchronous idle	54	36	6	86	56	V	118	76	v
23	17	End trans. block	55	37	7	87	57	W	119	77	w
24	18	Cancel	56	38	8	88	58	X	120	78	x
25	19	End of medium	57	39	9	89	59	Y	121	79	y
26	1A	Substitution	58	3A	:	90	5A	Z	122	7A	z
27	1B	Escape	59	3B	;	91	5B	[	123	7B	{
28	1C	File separator	60	3C	<	92	5C	\	124	7C	|
29	1D	Group separator	61	3D	=	93	5D	]	125	7D	}
30	1E	Record separator	62	3E	>	94	5E	^	126	7E	~
31	1F	Unit separator	63	3F	?	95	5F	_	127	7F	□

TABLE ASCII -II

Dec	Hex	Char	Dec	Hex	Char	Dec	Hex	Char	Dec	Hex	Char
128	80	Ç	160	A0	á	192	C0	└	224	E0	α
129	81	ü	161	A1	í	193	C1	┴	225	E1	ß
130	82	é	162	A2	ó	194	C2	┬	226	E2	Γ
131	83	â	163	A3	ú	195	C3	├	227	E3	π
132	84	ä	164	A4	ñ	196	C4	─	228	E4	Σ
133	85	à	165	A5	Ñ	197	C5	┼	229	E5	σ
134	86	å	166	A6	ª	198	C6	╞	230	E6	µ
135	87	ç	167	A7	º	199	C7	╟	231	E7	τ
136	88	ê	168	A8	¿	200	C8	╚	232	E8	Φ
137	89	ë	169	A9	⌐	201	C9	╔	233	E9	Θ
138	8A	è	170	AA	¬	202	CA	╩	234	EA	Ω
139	8B	ï	171	AB	½	203	CB	╦	235	EB	δ
140	8C	î	172	AC	¼	204	CC	╠	236	EC	∞
141	8D	ì	173	AD	¡	205	CD	═	237	ED	ø
142	8E	Ä	174	AE	«	206	CE	╬	238	EE	ε
143	8F	Å	175	AF	»	207	CF	╧	239	EF	∩
144	90	É	176	B0	░	208	D0	╨	240	F0	≡
145	91	æ	177	B1	▒	209	D1	╤	241	F1	±
146	92	Æ	178	B2	▓	210	D2	╥	242	F2	≥
147	93	ô	179	B3	│	211	D3	╙	243	F3	≤
148	94	ö	180	B4	┤	212	D4	╘	244	F4	⌠
149	95	ò	181	B5	╡	213	D5	╒	245	F5	⌡
150	96	û	182	B6	╢	214	D6	╓	246	F6	÷
151	97	ù	183	B7	╖	215	D7	╫	247	F7	≈
152	98	ÿ	184	B8	╕	216	D8	╪	248	F8	°
153	99	Ö	185	B9	╣	217	D9	┘	249	F9	∙
154	9A	Ü	186	BA	║	218	DA	┌	250	FA	·
155	9B	¢	187	BB	╗	219	DB	█	251	FB	√
156	9C	£	188	BC	╝	220	DC	▄	252	FC	ⁿ
157	9D	¥	189	BD	╜	221	DD	▌	253	FD	²
158	9E	₧	190	BE	╛	222	DE	▐	254	FE	■
159	9F	ƒ	191	BF	┐	223	DF	▀	255	FF	