E-DDC™

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VESA Enhanced Display Data Channel (EDDC) Standard

Version 1.2

December 26, 2007

Purpose

The purpose of this standard is to define a communications channel between an electronic display (e.g. a CRT, LCD, etc display) and a host system. The channel may be used to carry configuration information to enable 'plug & play' and allow optimum use of the display. The channel may also carry display control information.

Summary

Today's computing and consumer electronic environments demands that systems offer user-friendly set-up. With the growing popularity of intuitive and simpler software user interfaces, hardware manufacturers are responding with plug-and-play systems and peripherals. However, for the user to receive full benefit from these advances, standardization is necessary. VESA, as the prominent standards organization for graphics subsystems, has developed a communications channel between the host and the display. This communication channel offers basic configuration information plus a standard way of communicating advanced functionality

Errata or SCRs published

Adopted April 19, 2013: E-DDC Address Update NXP v2

1 Summary of the Proposed Change(s) for E-DDC Address Update SCR

The list of devices that can be connected to the same I²C / DDC bus doesn't reflect all the modules we have today on DDC bus in HDMI and DisplayPort systems.

1.1 IPR (Intellectual Property Rights) declaration, if any

N/A

1.2 Benefits as a Result of the Changes

Avoid conflict with other devices connected on the I²C / DDC bus.

1.3 Assessment of the Impact

It's just a clarification of slave addresses already allocated by other specifications using the Display Data Channel.

No change of features, protocol or electrical specification.

1.4 Analysis of the Device Hardware Implication

The hardware implementation is mandatory by the other specifications, so the slave address allocation is already done as soon as the product respects the features of the corresponding specification.

About conflict between Audio Processor and DisplayPort Dual-Mode Video Adaptor, these are not expected to co-exist on the same physical DDC bus in practice.

1.5 Analysis of the Device Software Implications

No software change is needed.

1.6 Analysis of the Compliance Test & Interop Implications

Already tested in different Compliance Tests (HDMI, HDCP, DP, DP Dual Mode).

1.7 New Referenced Documents Resulting from Change

1. High-bandwidth Digital Content Protection System Revision 1.4, July 2009.
2. VESA DisplayPort Dual-Mode Standard Version 1, February 2012.
3. High-Definition Multimedia Interface specification Version 2.0, March 2013.
4. Display Data Channel Command Interface Standard Version 1.1, Oct 29, 2004.

2 Proposed Document Change(s) or Addition(s)

This section captures the list of proposed document changes in the specification.

2.2.2 Display Data Channel (DDC)

A protocol based on I^2C and used on a bi-directional data channel between the display and host. This protocol accesses devices at I^2C addresses of A0h / A1h or A4h / A5h.

The DDC channel is used by HDMI, DP and DisplayPort Dual Mode standards for purposes beyond EDID data transport. The I^2C slave/device addresses used by these standards are listed in Table 2-2. The intended purposes of these addresses are described in those respective standards.

2.2.3 DDC addresses ~~(A0h / A1h and A4h / A5h)~~

Under DDC, each pair of I^2C slave addresses (A0h/A1h and A4h/A5h) allows 256 bytes of data to be accessed. Larger data structures, up to 32K bytes, can be accessed using the E-DDC addressing technique – see section 2.2.4.

2.2.3.1 Other DDC addresses

Table 2-2 lists the DDC/I^2C addresses that are defined by DDC, HDMI, DP and DisplayPort Dual Mode standards.

Table 2-2: Normative Addresses

I^2C Slave Address	Specification
0x74h/75h	Reserved for HDCP (Primary Link Port) [1]
0x76h/77h	Reserved for HDCP (Secondary Link Port) [1]
0x80h/81h	Reserved for DisplayPort (Dual Mode Video Adaptor[2]
0xA8h/A9h	Reserved for HDMI[3]
0x6Eh/6Fh	Reserved for DDC/CI Display for host communication (e.g. MCCS)[4]

Note: Given that DisplayPort Dual Mode Video Adaptor uses the same Slave Address as that of Audio Processor, they can't co-exist on the same physical DDC bus.

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Preface

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Clarifications and application notes to support this standard may be written. To obtain the latest standard and any support documentation, contact VESA.

If you have a product that incorporates the Enhanced Display Data Channel (E-DDC), you should ask the company that manufactured your product for assistance. If you are a manufacturer, VESA can assist you with any clarification you may require. Submit all comments or reported errors in writing to VESA using one of the following methods.

- Fax: 510 651 5127, *direct this fax to Technical Support at VESA*
- e-mail: support@vesa.org
- Mail: Technical Support

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Acknowledgements

This document would not have been possible without the efforts of the VESA Display Systems Committee's EDDC Task Group. In particular, the following individuals and their companies contributed significant time and knowledge.

Table 1-1: Main Contributors to Version 1, Revision 2

Name	Company	
Syed Athar Hussain	AMD	
Ashley Saldanha	EnTech Taiwan	Task Group Chair
Ian Miller	Ian Miller Consultancy	Document Editor
Chandra Kondura	Intel	
Matt Sottek	Intel	
Christian Hofmann	Kontron	
Jim Webb	Xponent	Task Group Vice-chair
Alain d'Hautecourt	ViewSonic	

Revision History

Version 1 September 2, 1999

Initial release of the standard. The body of the standard is derived from the VESA DDC Version 3 Standard. The major changes were the addition of the E-DDC protocols, removal of DDC1 protocol and clarification to the DDC power requirements.

Version 1, Revision 1 March 24, 2004

A revision and update to the E-DDC standard to encompass usage in consumer electronic products and video interfaces other than VGA, with text clarified in several places.

Version 1, Revision 2 December 26, 2007

This revision updates the E-DDC standard, expanding its scope to encompass DisplayID and DisplayPort, and correcting and clarifying text in several places.

1. OVERVIEW

1.1 Summary

The Display Data Channel, DDC, is a subset of the I^2C bus used to provide bi-directional communications between a host device and an attached display. In their basic form, the capabilities are limited to allowing the host to request and read the EDID or the DisplayID from the display – EDID and DisplayID are alternate structures that each contains information about the capabilities of the display.

In the DDC standard, the host could only access a very limited address space which constrained the size of the EDID or DisplayID. E-DDC is fully backward compatible with DDC, but enables a significantly larger address space to be used.

Notes:

1) The content and format of EDID are not defined in this standard; refer to the VESA Enhanced Extended Display Identification Data Standard (E-EDID) and, where appropriate, the various VESA E-EDID extension block standards and the CEA E-EDID extension defined in the CEA-861 standard.
2) The content and format of DisplayID are not defined in this standard. Refer to the VESA Display Identification (DisplayID) Standard.

The scope of this document is to provide a detailed description of the operation of E-DDC and its implementation.

However, in addition to serving to request and transmit EDID and DisplayID, the Display Data Channel also allows more advanced communication between the display and host. This enables the host to control many aspects of the display capabilities and functions. For details of this communication mode see the VESA Display Data Channel Command Interface Standard (DDC/CI) and for details of commands see the VESA Monitor Command and Control Set (MCCS) standard.

Note: The "monitor" in the MCCS name should not be taken to mean that it only applies to computer displays; many MCCS commands are applicable to any electronic display and some are exclusively for television purposes.

DDC communications has been widely implemented in a number of video interfaces including VGA (15 pin high-density D-sub), DVI and HDMI. Support is also provided in the VESA DisplayPort standard via emulation.

This document does not specify how the E-DDC interfaces communicate to the host CPU and GPU address and I/O spaces.

Earlier versions of the DDC and E-DDC standards introduced and supported a very simple unidirectional, display to host, DDC1 mode – this mode is no longer supported by VESA.

The VESA task group responsible for the development of this standard has spent considerable time considering how best to manage the situation where there are two (EDID and DisplayID) schemes that may be used to convey capability information from the display to the host. The conclusion can be summarized as follows:

- The data at I^2C slave addresses A0h / A1h will be the primary location for display capability information.
- A second pair of I^2C slave addresses at A4h / A5h will be the secondary location for display capability information.

Further details are contained in Section 3.

1.2 Background

Early personal computer monitor identification schemes were only capable of handling a limited number of display types and parameters. Since these schemes carried very little information about the capabilities of the display, they were of limited value.

Earlier versions of DDC and EDID defined a communication method and configuration data appropriate for traditional CRT displays, but were limited in their support of other display types and the amount of data that could be supported in the display. Over time, VESA introduced enhanced versions of the DDC and EDID standards, E-DDC and E-EDID respectively, with new capabilities.

As new display technologies have been introduced to the market, support for communication methods and configuration information suitable for these displays has become a necessity. In recent years displays intended for digital and high definition television have also adopted DDC communication to transfer EDID from the display to the host.

DisplayID is a new (2007) standard which has a number of advantages expected to coexist with EDID for some time. Some products may have either an EDID or a DisplayID, depending on the market. Others may implement both EDID and DisplayID within a single display.

DisplayID advantages:

- Modular
    - The manufacturer selects which blocks are appropriate for the product
- Flexible block size
    - Many of the block definitions have variable lengths so that they can be used or either simple or advanced display capabilities
- Efficient
    - Block types and size are matched to the requirements of the individual display type.
    - Overall size is determined by the product requirements.
- No assumption about display technology
    - No implicit assumptions about the display technology being used.

Note: For convenience and compatibility with EDID structures, it is implied in this document that DisplayID is organized in 128 byte blocks. However, DisplayID actually has a variable length – see DisplayID standard for details. The techniques described here will work, but may not be the most efficient when applied to DisplayID.

1.3 Significant Changes in Current E-DDC Revision

This revision (1.2) updates the E-DDC standard with clarification and corrections together with support for DisplayID. Changes may be summarized as:

- No support for the DDC1 mode of operation
- Clarification of the use of DDC on multiple interfaces – VGA, DVI, HDMI and DisplayPort
- Addition of a compliance section – section 10
- Deletion of notes regarding possible move from +5V to +3.3V for DDC power
- Support for DisplayID added.

1.4 Reference Documents

Versions identified here are current but users of this standard are advised to ensure they have the latest versions of reference standards and documents.

Table 1-1: Reference Documents

Document	Version / Revision	Date
VESA Glossary of Terms – see www.vesa.org	Current	Current
VESA Policy 200, Intellectual Property Rights	B	December 2004
VESA Video BIOS extensions for Display Data Channel (VBE/DDC)	Version 1 / Revision 1	November 1999
VESA Enhanced Extended Display Identification Data (E-EDID)	Version A / Revision 2	September 2006
VESA Monitor Command and Control Set (MCCS)	Version 3	July 2006
VESA Display Data Channel – Command Interface (DDC/CI)	Version 1 / Revision 1	October 2004
VESA Plug & Play (PnP) Standard for the Display/Graphics Subsystem	Release A	June 2004
VESA E-EDID Localized String Extension (LS-EXT™) Standard	Release A	July 2003
VESA Display Color Management (DCM™) Standard	Version 1	January 2003
VESA Display Information Extension (DI-EXT™) Block Standard	Release A	August 2001
VESA Display Identification (DisplayID) Standard	Version 1	December 2007
VESA DisplayPort Standard	Version 1 / Revision 1	March 2007
The I^2C Bus Specification	Version 2.1	January 2001
Microsoft Plug and Play for Windows 2000 and Windows XP	White Paper	December 2001
IBM Personal System/2 Hardware Interface Technical Reference - Common Interfaces	First Edition	1987
CEA-861 Standard, A DTV Profile for Uncompressed High Speed Digital Interfaces	D (or newer)	2006
Digital Visual Interface (DVI)	Revision 1.0	April 1999
High-Definition Multimedia Interface (HDMI)	Version 1.3	June 2006
High-bandwidth Digital Content Protection Scheme (HDCP)	Version 1.3	December 2006

2. DEFINITIONS

In the following sections and unless otherwise specified "EDID" refers to all revisions of EDID Version 1, up to and inclusive of the latest revision - see the latest VESA E-EDID standard for details.

2.1 Data formats

2.1.1 Enhanced Extended Display Identification Data: E-EDID

The E-EDID standard defines a 128 byte EDID structure containing the display identity and the basic display specifications. It also defines support for a number of 128 byte extensions which allow additional information to be communicated.

2.1.2 Enhanced Extended Display Identification Data Extension Blocks

A number of VESA standards have been approved which define EDID extension blocks, see the reference document list.

Note: New extension block standards are likely to be developed; check the VESA website for the latest standards.

The CEA has also developed an EDID Timing Extension Block for use by digital television products compliant with the CEA-861 specification.

2.1.3 Display Identification: DisplayID

The DisplayID standard defines a number of blocks and an overall framework. The DisplayID framework is of variable length and is formed by selecting the appropriate blocks and the appropriate level of detail within each of the variable length blocks to describe the capabilities of the display.

2.2 Communication Protocols

The original DDC standard supported two modes, a very simple mode called DDC1 and an I^2C bus based mode called DDC2.

Several terms have been used for versions of DDC2 with different features and capabilities; these are summarized in Table 2-1.

Table 2-1: Summary of DDC Communication Modes

Name	Purpose	Comment
DDC	Display Data Channel	Generic term
DDC1	Original unidirectional mode (display → host)	Not supported by VESA
DDC2	Original bi-directional mode. Host able to request EDID data	Not supported by VESA
DDC2B	A generic term for all bi-directional DDC modes	Not supported by VESA
DDC2Bi	Original name for command interface mode	Old terminology, replaced by DDC/CI
E-DDC	Enhanced DDC, a bi-directional mode, supporting access to EDID data including all possible EDID extension blocks	Recommended for all new display designs
DDC/CI	The command interface uses I^2C single master communications and allows MCCS VCP codes and associated data to be sent to or received from a display	Recommended for new display designs when support for the MCCS VCP codes is required.

Notes:

a) E-DDC is the base level of support recommended for all new display designs. Some designs will

choose to implement DDC/CI to provide additional functions.

b) DDC/CI does not replace the need for E-DDC support; DDC/CI provides an extension to E-DDC.

c) The terminology on a gray background in Table 2-1 should not be used.

2.2.1 I^2C Bus

A standard protocol two-wire (clock and data) serial data bus. See I^2C specification for details.

Notes:

1) All display devices on an I^2C bus are allocated fixed, slave addresses
2) The primary I^2C slave addresses for display capability information are A0h / A1h. A display which does not support any form of display capability information should NAK any read / write to these addresses.
3) The secondary I^2C slave addresses for display capability information are A4h / A5h. A display which does not support secondary display capability information should NAK any read / write to these addresses.

2.2.2 Display Data Channel (DDC)

A protocol based on I^2C and used on a bi-directional data channel between the display and host. This protocol accesses devices at I^2C addresses of A0h / A1h or A4h / A5h.

2.2.3 DDC addresses (A0h / A1h and A4h / A5h)

Under DDC, each pair of I^2C slave addresses allows 256 bytes of data to be accessed. Larger data structures, up to 32K bytes, can be accessed using the E-DDC addressing technique – see section 2.2.4.

2.2.4 Enhanced DDC (E-DDC)

A protocol based on I^2C and used on a bi-directional data channel between the display and host. This protocol accesses devices at I^2C addresses of A0h / A1h or A4h / A5h used in conjunction with a register at address 60h.

The 60h address is used as a segment pointer register; see section 2.2.5 to allow larger amounts of data to be retrieved than is possible using DDC. This mode is backwards compatible with DDC.

Note: The segment pointer register is shared by both the primary and secondary display capabilities I^2C slave addresses.

2.2.5 Segment pointer (60h)

E-DDC allows access of up to 32 Kbytes of data. This is accomplished using a combination of the A0h / A1h or A4h / A5h address pair and a segment pointer.

The segment pointer acts as an adjustable offset so that the address pair A0h / A1h or A4h / A5h can be used to access many different 256 byte blocks. This is shown graphically in Figure 2-1.

The segment pointer is a one byte value at address 60h. If the segment pointer is set = 0 the commands using addresses A0h / A1h or A4h / A5h will access blocks 0 and 1 respectively which are the first two 128 byte blocks in the EDID or DisplayID memory space.

Notes:

a) The default value in the segment pointer is zero. This ensures backward compatibility with DDC

operation.

b) For completeness and consistency, there are several instances where "set the segment pointer = n" occurs in this document, where "n" represents any integer value. Since the segment pointer, however, is always reset to zero at power on and after each use, this instruction is redundant except when a non-zero value of the segment pointer is required.

Each successive value of the segment pointer allows access to the next two 128 byte blocks in the display capability memory space.

Notes: The segment pointer register is effectively a "write only register" since it is reset to zero (the default value) at the completion of each command sequence. In this context a "command sequence" is:

a) A write operation to load the appropriate value in the segment pointer, and

b) A read operation(s) to transfer the EDID or DisplayID selected by the combination of the segment pointer value and a display capability slave address.

2.2.6 Typical Operation Sequences

The following are typical but other command sequences are possible depending on the implementation specifics, e.g., some implementations may support auto-incrementing beyond the 128 byte boundary allowing a single sequential read operation to access 256 bytes of data.

Two examples are given:

1) A DDC operation to read a base EDID plus one extension block, i.e. 256 bytes of data; see section 2.2.6.1

   Note: Under DDC 256 bytes of data is the maximum possible.

2) An E-DDC operation to read a base EDID plus four extension blocks, i.e. 640 bytes of data; see section 2.2.6.2

2.2.6.1 DDC Operation

This is a typical command sequence required to read an EDID structure that contains the base EDID plus one extension block, i.e. a total of 256 bytes of data.

- DDC sequential read of first 128 bytes – refer to section 6.3
  - Word offset = 00h
- DDC sequential read of second 128 bytes – refer to section 6.3
  - Word offset = 80h

2.2.6.2 E-DDC Operation

Refer to Figure 2-1.

This is a typical command sequence required to read an EDID structure that contains the base EDID plus an extension block map plus four extension blocks, i.e. a total of 640 bytes of data.

- E-DDC sequential read of first 128 bytes – refer to section 6.5
  - Segment pointer and word offset = 00h
- E-DDC sequential read of second 128 bytes, the extension block map – refer to section 6.3
  - Segment pointer set = 0 and word offset = 80h

- E-DDC sequential read of third 128 byte block, the first “true” EDID extension – refer to section 6.5
  - Segment pointer = 1 and word offset = 00h
- E-DDC sequential read of fourth 128 byte block, the second “true” EDID extension – refer to section 6.5
  - Segment pointer = 1 and word offset = 80h
- E-DDC sequential read of fifth 128 byte block, the third “true” EDID extension – refer to section 6.5
  - Segment pointer = 2 and word offset = 00h

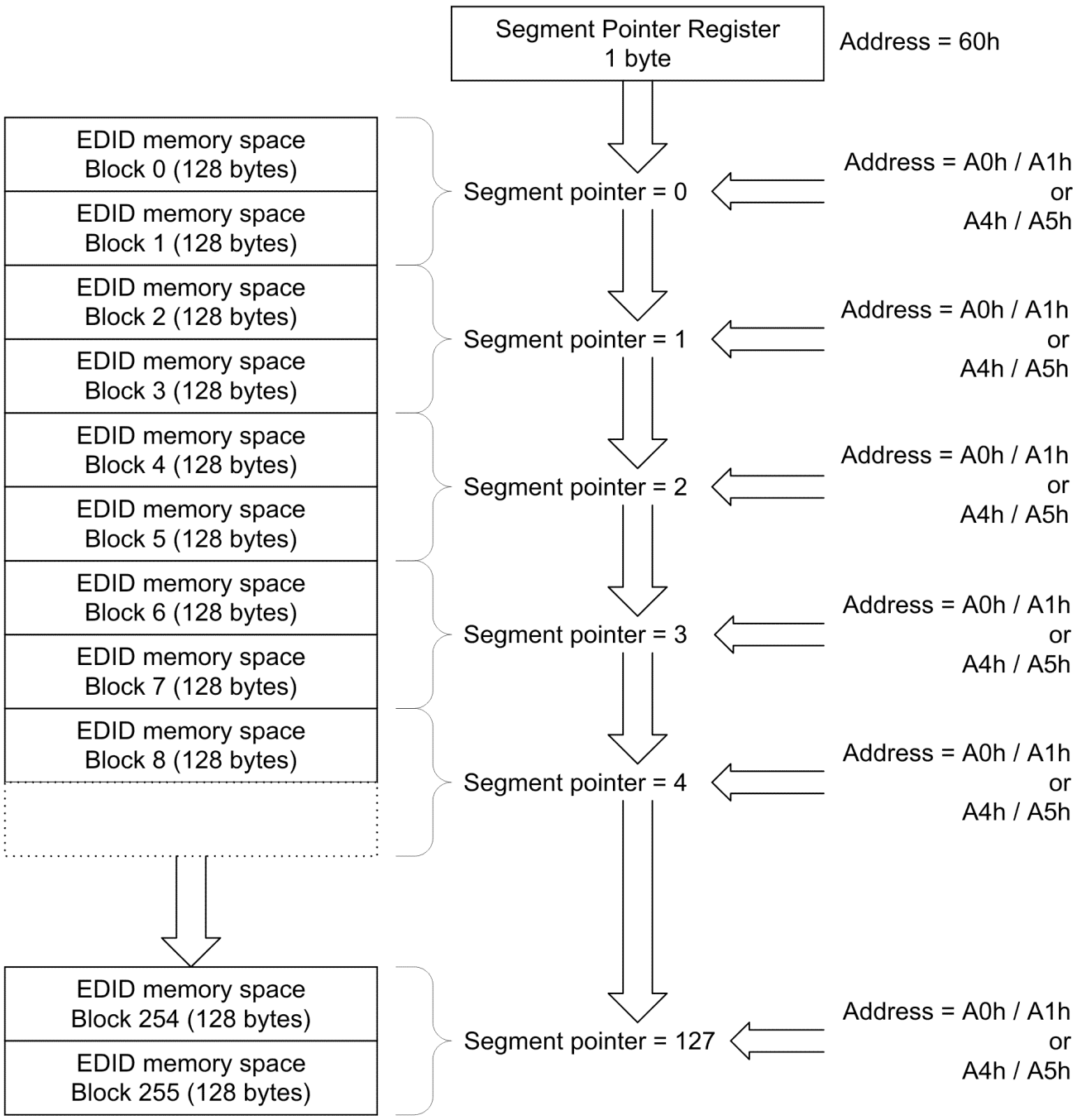


Figure 2-1: E-DDC Segment Pointer and Block Layout

2.2.7 DDC Command Interface (DDC/CI)

An extension of the DDC mode used for interactive control of the display by the host. The protocols provide a mechanism to send any of a wide range of commands to the display, many of which have associated data which may be sent to the display or received from the display. See the VESA DDC/CI and MCCS standards for details.

2.3 Display Types

Refer to section 3 for rules governing the coexistence of EDID and DisplayID structures.

2.3.1 Non-DDC Display

- Display with no DDC capabilities – this is very unusual now except for televisions with no external digital interface.

2.3.2 DDC Display

- DDC capable
- Display contains EDID data (128 bytes) and, optionally, an EDID Extension block (128 bytes) at I^2C address A0h / A1h

  Or,

- Display contains EDID data (128 bytes) and, optionally, an EDID Extension block (128 bytes) at I^2C address A0h / A1h, and a DisplayID (variable length to maximum of 256 bytes) at I^2C address of A4h / A5h

2.3.3 Enhanced DDC Display

- Supports E-DDC addressing with a segment pointer register at 60h.
- Display with EDID 1.3 (or higher) data and up to 255 extension blocks of 128 bytes each (up to 32K bytes total EDID memory) at I^2C address A0h / A1h

Or,

- Display contains a DisplayID (variable length) of up to 32K bytes at I^2C address A0h / A1h

Or,

- Display contains EDID 1.3 (or higher) data and up to 255 extension blocks at I^2C address A0h / A1h and a DisplayID (variable length to maximum of 32K bytes) at I^2C address of A4h / A5h

2.4 Host System Types

2.4.1 Non-DDC Host

- Host without DDC capabilities – this is very unusual now except for consumer electronic hosts (set top box, DVD player, etc) that have no external digital interface.

2.4.2 DDC Host

- Host using DDC protocols
  - Read up to 256 bytes from the primary location for display capability information at A0h / A1h.

- May be able to read up to 256 bytes from the secondary location for display capability information at A4h / A5h.

2.4.3 E-DDC Host

- Host using Enhanced DDC protocols including writing to a segment pointer to access display capability memory spaces.
  - Reads EDID data from a display capability memory block defined by the combination of the segment pointer value and I^2C address A0h / A1h
  - Reads E-EDID extensions from a display capability memory block defined by the combination of the segment pointer value and I^2C addresses A0h and A1h.

  And / or,

  - Reads DisplayID (variable length) from a display capability memory block defined by the combination of the segment pointer value and I^2C addresses A0h / A1h or A4h / A5h.

3. Co-existance of EDID and DisplayID Display Capability Structures

With the introduction of DisplayID, the system level requirement to access the available display capability structure(s) becomes more complex but two simple rules ensure:

- Backward compatibility
- A predictable coexistence of EDID and DisplayID when appropriate
- Manufacturers have the option to include either or both EDID and DisplayID structures with confidence that their product will interoperate with others in the market.

Rules:

1) If only an EDID display capability structure is present then it must be at I^2C slave addresses A0h / A1h – the primary location for display capability information.
2) If a product contains both EDID and DisplayID display capability structures then the EDID must be at I^2C address A0h / A1h and the DisplayID must be at A4h / A5h.

If a product only supports a DisplayID structure, the DisplayID data must be at I^2C address A0h / A1h – the primary location for display capability information. Display manufacturers should be aware that this will result in a "plug and play" failure with host devices that expect an EDID at I^2C address A0h / A1h.

3.1 Example of Host Operation

A possible operating scheme for a host device:

- Read from address A0h
- Check that valid data has been received – use checksum.

  Note: In the case of DisplayID the checksum is at a variable location but a fixed location byte in each section header defines the length of that section (maximum 256 bytes) and the final byte is the checksum byte. See the DisplayID standard for details.
- If data is not valid, retry or exit to default situation.
- Parse data to determine if it is EDID or DisplayID.
- If EDID data then the host may read at address A4h to see if DisplayID is also available.
- Use display capability data to optimize system.

4. DDC/E-DDC - General

4.1 Signal Termination

The following are recommended for reliable operation:

1) Host devices should provide pull-up resistors of ≥ 1.5 KΩ and ≤ 2.2 KΩ to a +5 volt reference or a 3mA current source for the SCL and SDA open drain signals.
2) All the SDA and SCL pull up resistors should be located within the host system except for a 47 KΩ pull up resistor on the SCL line in the display.

4.2 Timing

4.2.1 DDC / E-DDC Timing

Data is synchronized with the clock signal and timing must comply with the I^2C specification. Refer to I^2C specification for details.

4.2.2 EDID Availability

The display must be capable of providing EDID over the DDC or E-DDC channel whenever the DDC +5 V or AUX_PWR +3.3 V signal is present (VGA pin # 9, DVI pin # 14, HDMI-A pin # 18, HDMI-B pin # 28, DisplayPort internal connector pin # 30) as appropriate). EDID must be available within 20 ms from the time when the +5 volt or +3.3 volt power (as appropriate) is present.

5. Data Transfer Protocols

5.1 DDC and E-DDC

DDC is a serial communications channel between the display and host operating in master – slave mode. The host is the 'master' and the display is the 'slave'.

The host uses I^2C commands structures to read EDID and an EDID extension (if present) or a DisplayID from the display using slave addresses of A0h / A1h or A4h / A5h.

E-DDC uses the same command structure with one addition. A segment pointer is used to allow addressing outside of the normal 256 byte limit of the A0 / A1h or A4h / A5h addresses. The E-DDC protocol writes the appropriate value into the segment pointer register before the remainder of the DDC command.

Table 5-1: DDC and E-DDC Device Addresses - EDID

Display type	EDID base address	Data size	EDID extension address	Data size
DDC	Device: A0h Word offset 00h	128 bytes	Device: A0h Word offset 80h	128 bytes
E-DDC	Segment pointer: 00h Device: A0h Word offset 00h	128 bytes	Segment pointer: Range of 00h - 7Fh Device: A0h Word offset: 00h or 80h	128 bytes

Table 5-2: DDC and E-DDC Device Addresses - DisplayID

Display type	DisplayID address	Data size	DisplayID address	Data size
DDC	Device: A0h or A4h Word offset 00h	128 bytes	Device: A0h or A4h Word offset 80h	128 bytes
E-DDC	Segment pointer: 00h Device: A0h or A4h Word offset 00h	128 bytes	Segment pointer: Range of 00h - 7Fh Device: A0h or A4h Word offset: 00h or 80h	128 bytes

Note: As noted in Section 1.2, DisplayID has variable length – see DisplayID standard for details. The use of "128 bytes" in the above table is for convenience but the actual data size is implementation specific.

5.1.1 Basic operation for E-DDC access of EDID:

- Read EDID
  - SET Segment 0, device A0h, start address 00h, READ 128 bytes
  - IF no valid response

    THEN display does not support EDID.
  - IF extension flag (byte 126 of base EDID) is not equal to zero

    THEN EDID extension block(s) of 128 bytes each can be read at subsequent segments and start addresses

    e.g. A single optional EDID block can be read with the command:

    Segment 0, device A0h, start address 80h, read 128 bytes

5.1.2 Basic Operation for E-DDC Access of DisplayID:

- Read DisplayID
  - SET Segment 0, device A0h or A4h, start address 00h, READ 128 bytes
  - IF no valid response

    THEN display does not support DisplayID.
  - If there is a valid response, then:

    Check length of DisplayID structure, if DisplayID > 256 bytes then read remainder of structure using appropriate segment pointer register entries.

6. Command Structures

The I^2C specification should be read to obtain a full understanding of command structures; this section only provides an introduction.

DDC (excluding the superseded DDC1 mode) and E-DDC operations use the address pair A0h / A1h or A4h / A5h to access the EDID or DisplayID memory space.

Note: Although it is common to refer to A0h / A1h or A4h / A5h as ”addresses” or “an address pair” they are more than addresses, the seven most significant bits are the address and the least significant bit (lsb) defines whether a write or read operation is to be performed.

If the lsb of A0h / A1h or A4h / A5h is equal to 0 then a write operation is to be performed and if the lsb of A0h / A1h is equal to 1 then a read operation is to be performed. i.e. A0h and A4h specify write operations and A1h and A5h specify read operations.

Note: This standard does not require that displays support a write operation using address A0h or A4h, the decision on whether to support or write operation is left to the display developer.

As shown in section 2.2, E-DDC also uses a segment pointer register at address 60h to redirect the A0h / A1h or A4h / A5h addresses to different 256 byte blocks within the EDID memory space.

Sections 6.1 through 6.5 show the command structures for reads of a single byte or a sequence of bytes for both DDC and E-DDC operations. Except in the cases where the segment pointer is used to access data beyond the first 256 bytes contained in segment 0, there is no difference between a DDC and an E-DDC command structure.

6.1 Read at the Current Address

This is the simplest form of read operation. It may be used either to access the data at the default address or if a previous operation has defined an address that has not been reset yet.

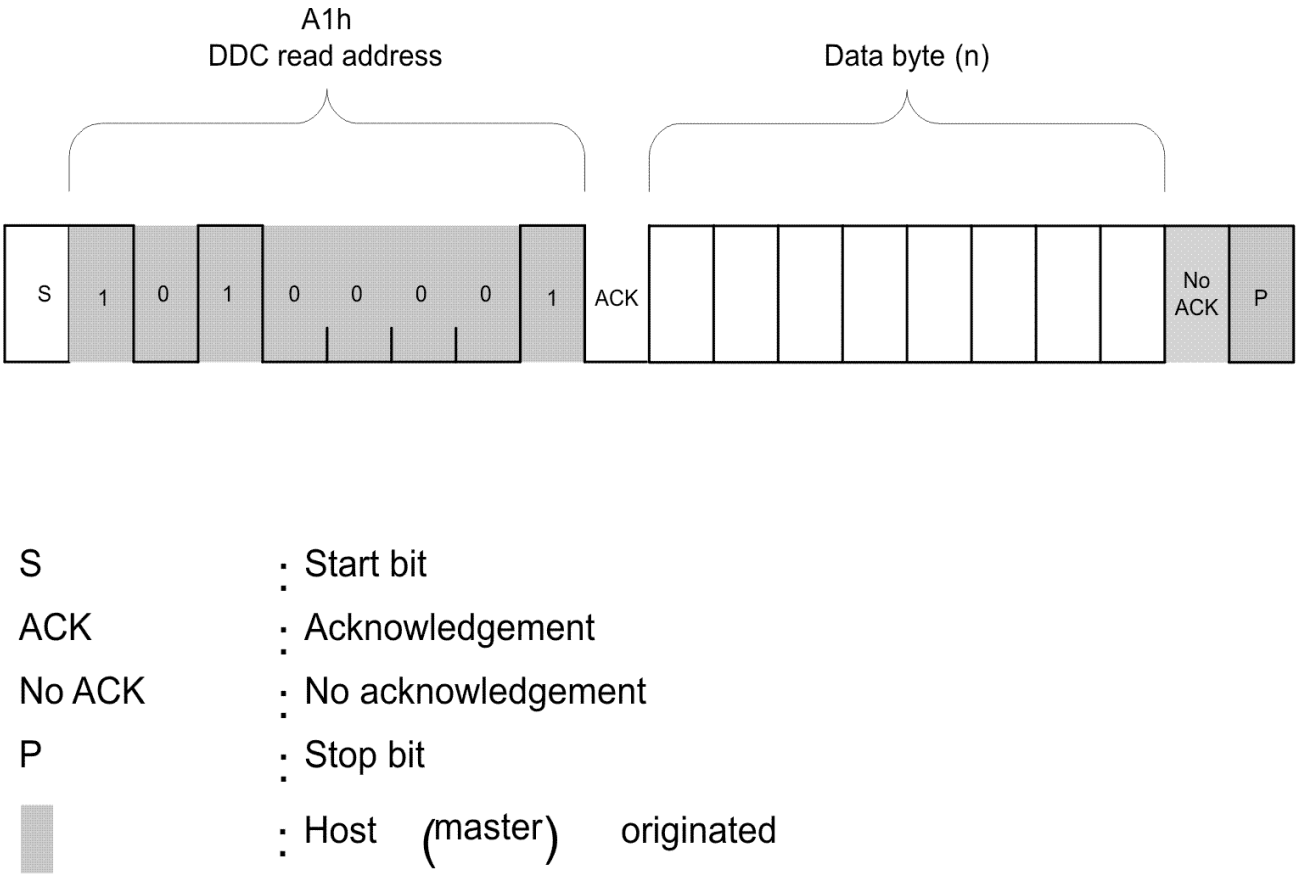


Figure 6-1: DDC Read at the Current Address

Note: Above example accesses the primary display capability memory space; to access the secondary display capability substitute A5h for A1h.

6.2 DDC Random Read Operation

This is the basic DDC read operation. The host initiates the transfer by writing the word offset (A0h) followed by a read (A1h) command, the display then responds with the data from the selected byte.

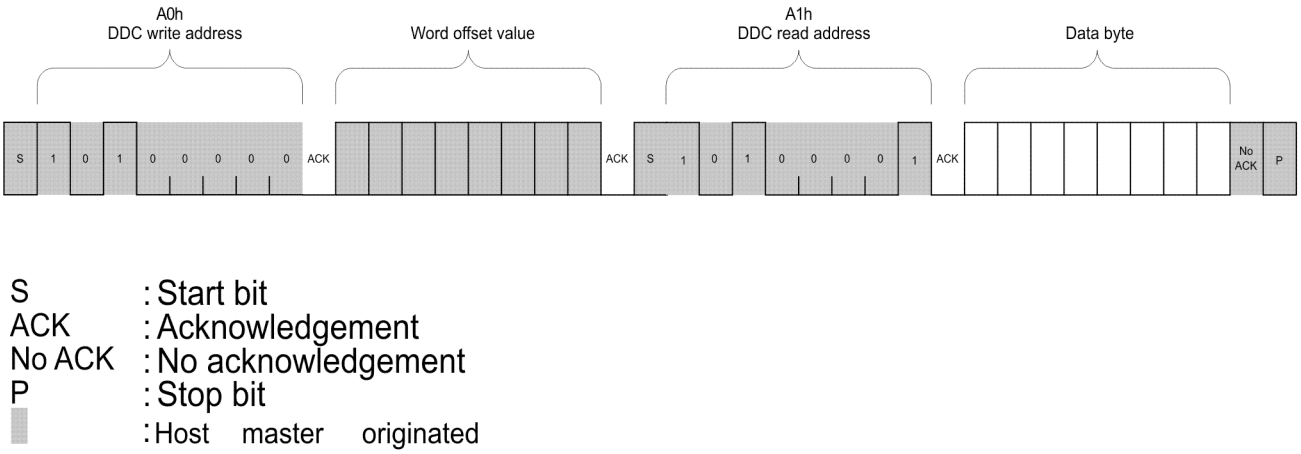


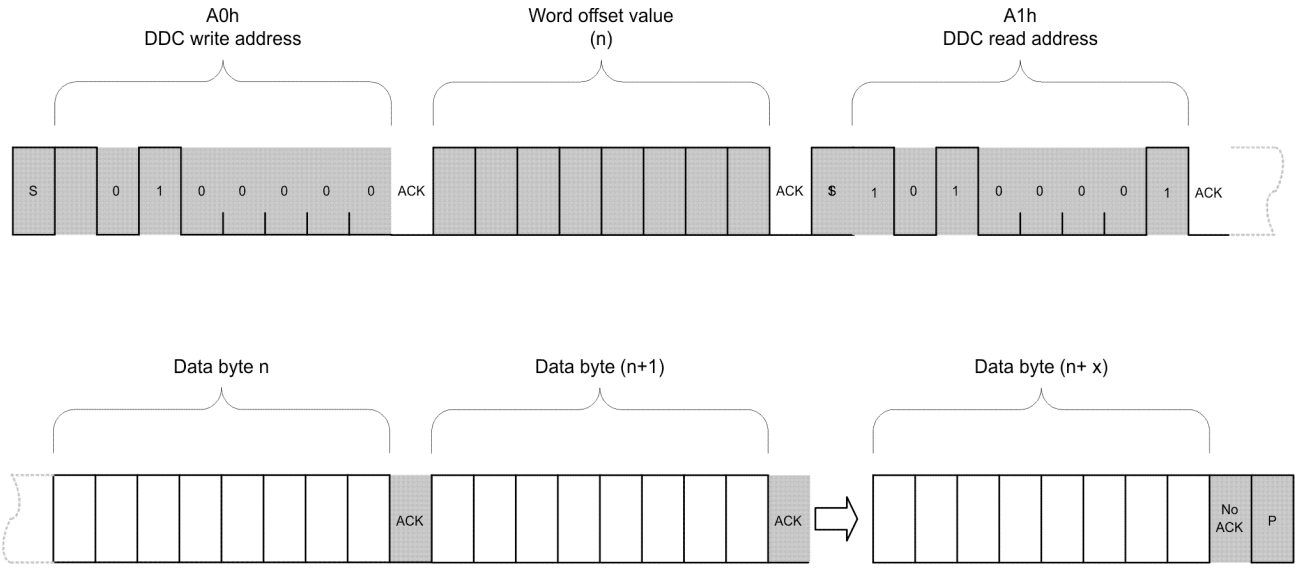
Figure 6-2: DDC Random Read Operation

Note: Above example accesses the primary display capability memory space; to access the secondary display capability substitute A5h for A1h and A4h for A0h.

6.3 DDC Sequential Read Operation

This is the most common DDC read operation. The host initiates the transfer by writing to the word offset (A0h) followed by a read command (A1h), the display then responds with a sequence of data bytes with the word offset auto incremented between successive bytes.

Note: In most cases the word offset will default to zero so that writing a word offset value is only required when the data required starts at an offset other than zero.



S : Start bit
ACK : Acknowledgement
No ACK : No acknowledgement
P : Stop bit
: Host (master) originated

Figure 6-3: DDC Sequential Read Operation

Note: Above example accesses the primary display capability memory space; to access the secondary display capability substitute A5h for A1h and A4h for A0h.

6.4 E-DDC Random Read Operation

This is the basic E-DDC read operation. It differs from the DDC random read operation (see section 6.2) only in respect of writing to the segment pointer register at address 60h at the start of the command structure.

The host initiates the transfer writing a value to the segment pointer register at address 60h. The host then writes the word offset (A0h) followed by a read (A1h) command, the display then responds with the data from the selected byte.

Note: The segment pointer is required to default to zero so that it is only necessary to use the complete command structure when reading data from segment 1 and higher.

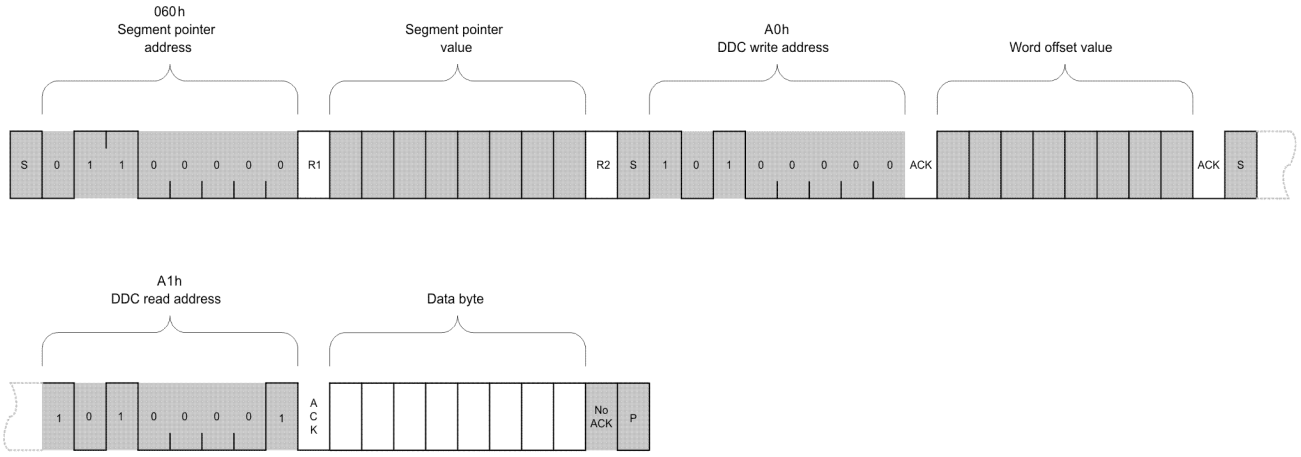


Figure 6-4: E-DDC Random Read Operation

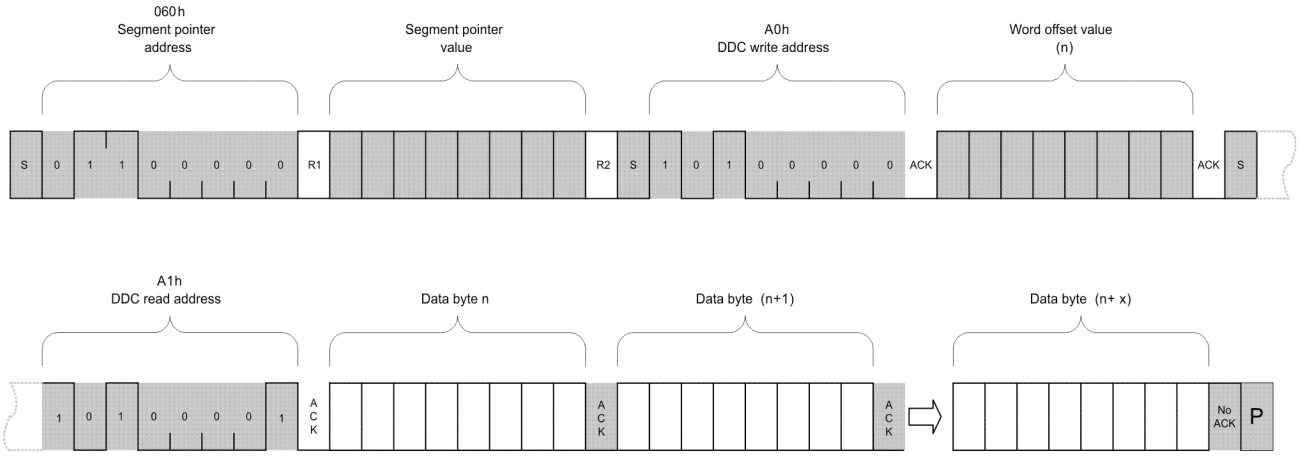
Note: Above example accesses the primary display capability memory space. To access the secondary display capability substitute A5h for A1h and A4h for A0h.

6.5 E-DDC Sequential Read Operation

Like the corresponding DDC sequential read (see section 6.3) this is the most common E-DDC read operation. It differs from the DDC sequential read operation only in respect of writing to the segment pointer register at address 60h at the start of the command structure.

The host initiates the transfer by writing a value to the segment pointer register at address 60h. The host continues the transfer by writing to the word offset (A0h) followed by a read command (A1h), the display then responds with a sequence of data bytes with the word offset auto incremented between successive bytes.

Note: The segment pointer is required to default to zero so that it is only necessary to use the complete command structure when reading data from segment 1 and higher.



S : Start bit
R1 : Do not care
R2 : Do not care for segment 0; ACK for segment 1 and higher
ACK : Acknowledgement
No ACK : No acknowledgement
P : Stop bit
: Host (master) originated

Figure 6-5: DDC Sequential Read Operation

Note: Above example accesses the primary display capability memory space; to access the secondary display capability substitute A5h for A1h and A4h for A0h.

7. Physical Connections – Video Interfaces

E-DDC and DDC/CI can be implemented on any video interface supporting the E-DDC standard. Examples include the 15 pin VGA, DVI and HDMI.

The VESA DisplayPort Standard also supports DDC via emulation such that the implementation details are different; see Sections 7.4 and 8.

The implementation details for the VGA interface are specified here. Basic implementation details for other interface standards are given here but the appropriate standard should be read to ensure the latest information is being used for these interfaces.

Note: In the event of a conflict between the information here and that contained in the standard for the relevant interface, the contents of the standard must be considered correct.

7.1 VGA

7.1.1 Mechanical

The mechanical specification for the DDC or E-DDC connector is backward compatible with the standard 15-position VGA-type connector with the following exceptions:

a) Socket # 9 must be recessed by 0.050 inches.

b) The host side connector color, plastic part, must be “royal blue” to clearly indicate that socket is DDC or E-DDC compatible.

Suitable connectors are available from a number of sources; the following are listed for reference.

Note: This does not imply that VESA recommends or approves these particular connectors:

- AMP p/n 787066-1 787066-2 787506-1
- Molex p/n 89263-*7** 89141-70** 89046-70**
-

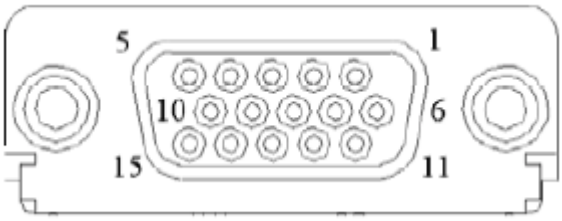


Figure 7-1: VGA Socket

7.1.2 VGA Connector Pinouts

Table 7-1: 15-pin D-type Connector Pinouts

Pin #	Legacy VGA	DDC / E-DDC Host	DDC / E-DDC Display
1	Red video	Red video	Red video
2	Green video	Green video (see note # 1)	Green video (see note # 1)
3	Blue video	Blue video	Blue video
4	Monitor identification bit 2	Monitor identification bit 2	Reserved - No connection
5	Test (ground)	Return (ground)	Return
6	Red video return	Red video return	Red video return
7	Green video return	Green video return	Green video return
8	Blue video return	Blue video return	Blue video return
9	No connection (mechanical key)	DDC +5 volt supply (required, see section 7.1.3.1)	DDC +5 volt load (see section 7.1.3.2)
10	Synchronization return	Synchronization return	Synchronization return
11	Monitor Identification bit 0	Monitor Identification bit 0	Reserved - No connection
12	Monitor Identification bit 1	Serial data (SDA)	Serial data (SDA)
13	Horizontal synchronization	Horizontal synchronization (see note # 2)	Horizontal synchronization (see note # 2)
14	Vertical synchronization	Vertical synchronization	Vertical synchronization
15	Monitor Identification bit 3	Serial clock (SCL)	Serial clock (SCL)

Notes:

1) This line may carry synchronization on green (SOG) signal if SOG is supported by both the display (indicated in the base EDID block) and the host.

2) This line may carry a composite synchronization signal when supported by both the display (indicated in base EDID block) and the host.

7.1.3 Power requirements

7.1.3.1 Host

All host devices, including battery powered devices, must supply +5 volts (+/- 5%) on pin # 9 whenever the video port is active. The required current capability is 50mA with over current protection to limit the maximum current to a maximum of one ampere.

7.1.3.2 Display

When the display is not AC powered and / or the power switch is in the off position, the display may draw up to 50mA at +5 volts from pin # 9.

When the display is AC powered and the power switch is the on position, the display must not draw more than 1mA at +5 volts from pin # 9.

7.2 Digital Visual interface (DVI)

Note: This information is provided for information only. User is advised to verify accuracy by checking the

latest revision of the DVI specification – in the event of conflict, the DVI specification must be considered correct.

7.2.1 Mechanical

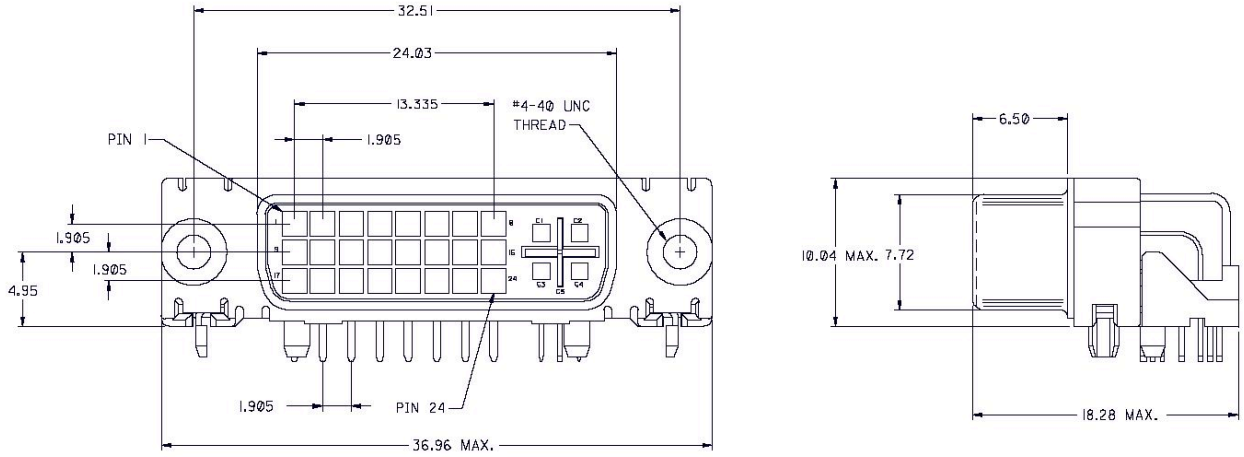


Figure 7-2: DVI -I Socket Drawing

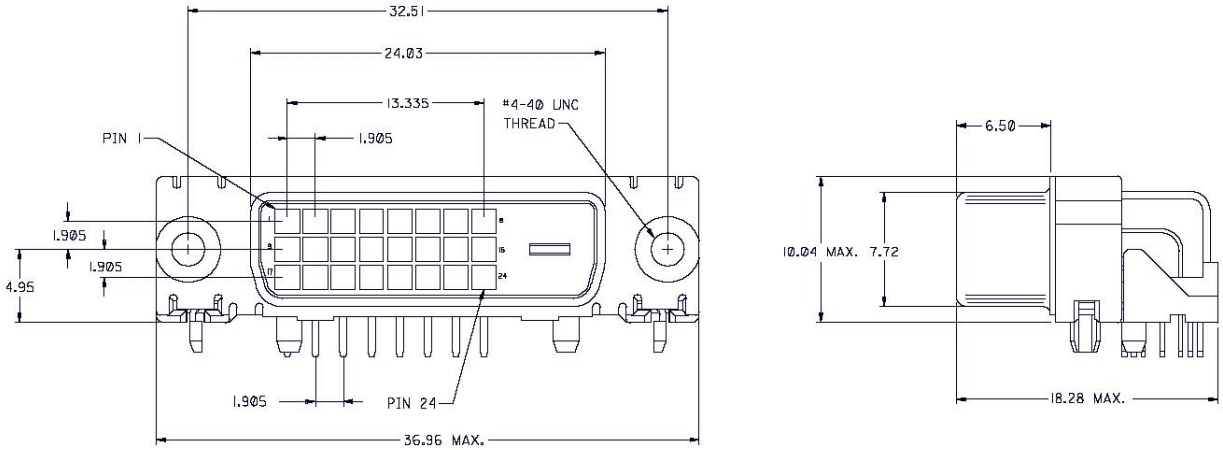


Figure 7-3: DVI-D Socket Drawing

7.2.2 Connector Pin-out

Table 7-2: DVI Connector Pin-out

Pin number	Signal	Pin number	Signal
1	TMDS data 2-	C1	Analog red
2	TMDS data 2+	C2	Analog green
3	TMDS data 2 / 4 shield	C3	Analog blue
4	TMDS data 4-	C4	Analog horizontal synchronization
5	TMDS data 4+	C5	Analog ground (red, green & blue returns)
6	DDC clock		
7	DDC data		
8	Analog vertical synchronization		
9	TMDS data 1-		
10	TMDS data 1+		
11	TMDS data 1 / 3 shield		
12	TMDS data 3-		
13	TMDS data 3+		
14	+ 5 volts		
15	Ground (synchronization & +5V returns)		
16	Hot plug detect		
17	TMDS data 0-		
18	TMDS data 0+		
19	TMDS data 0 / 5 shield		
20	TMDS data 5-		
21	TMDS data 5+		
22	TMDS clock shield		
23	TMDS clock-		
24	TMDS clock+		

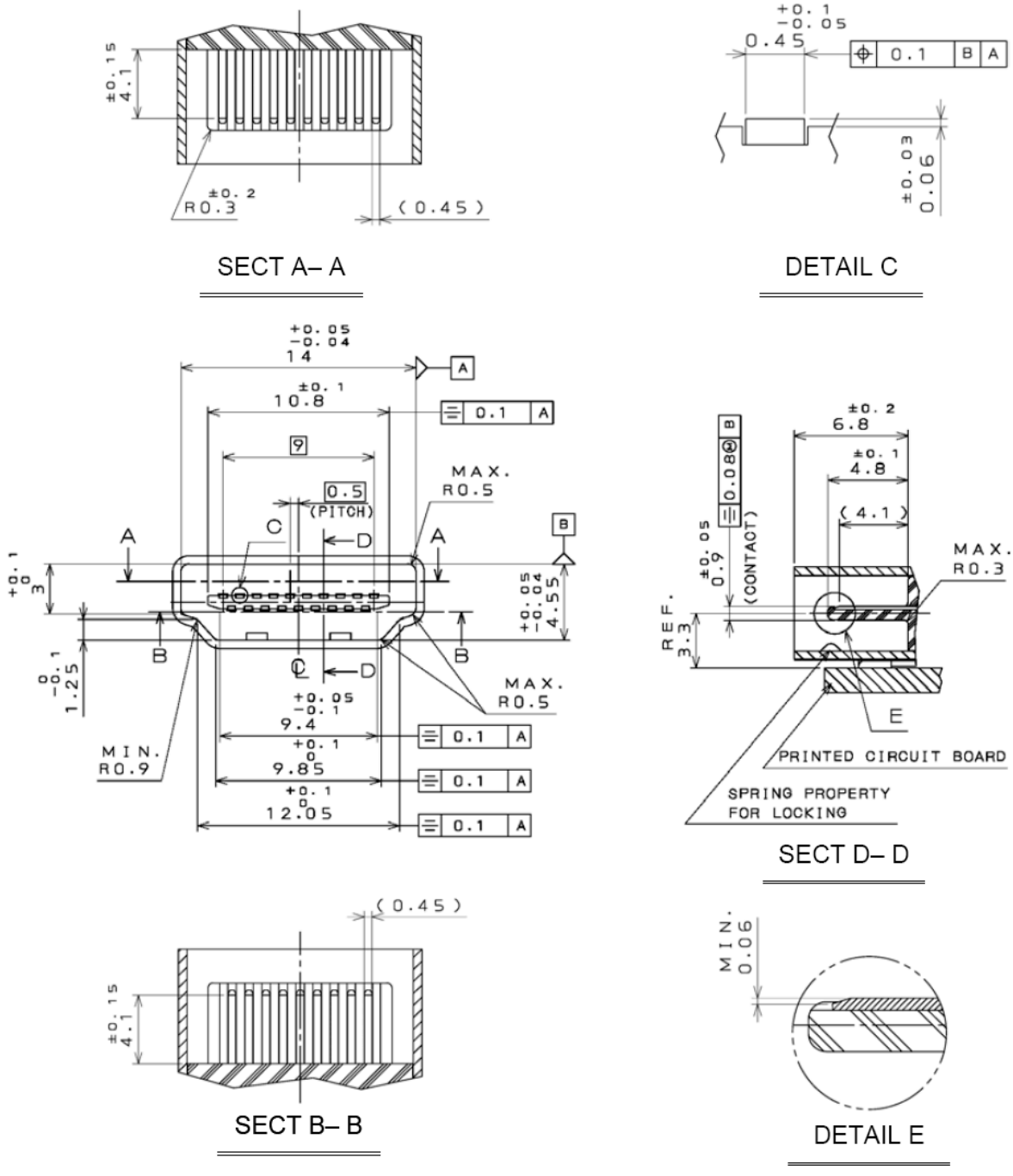
7.2.3 Power Requirements

Check the DVI specification for details of the voltage and current limits on the +5 volt line.

7.3 High Bandwidth Digital Multimedia Interface (HDMI)

Note: This information is provided for information only. User is advised to verify accuracy by checking the latest revision of the HDMI specification – in the event of conflict, the HDMI specification must be considered correct.

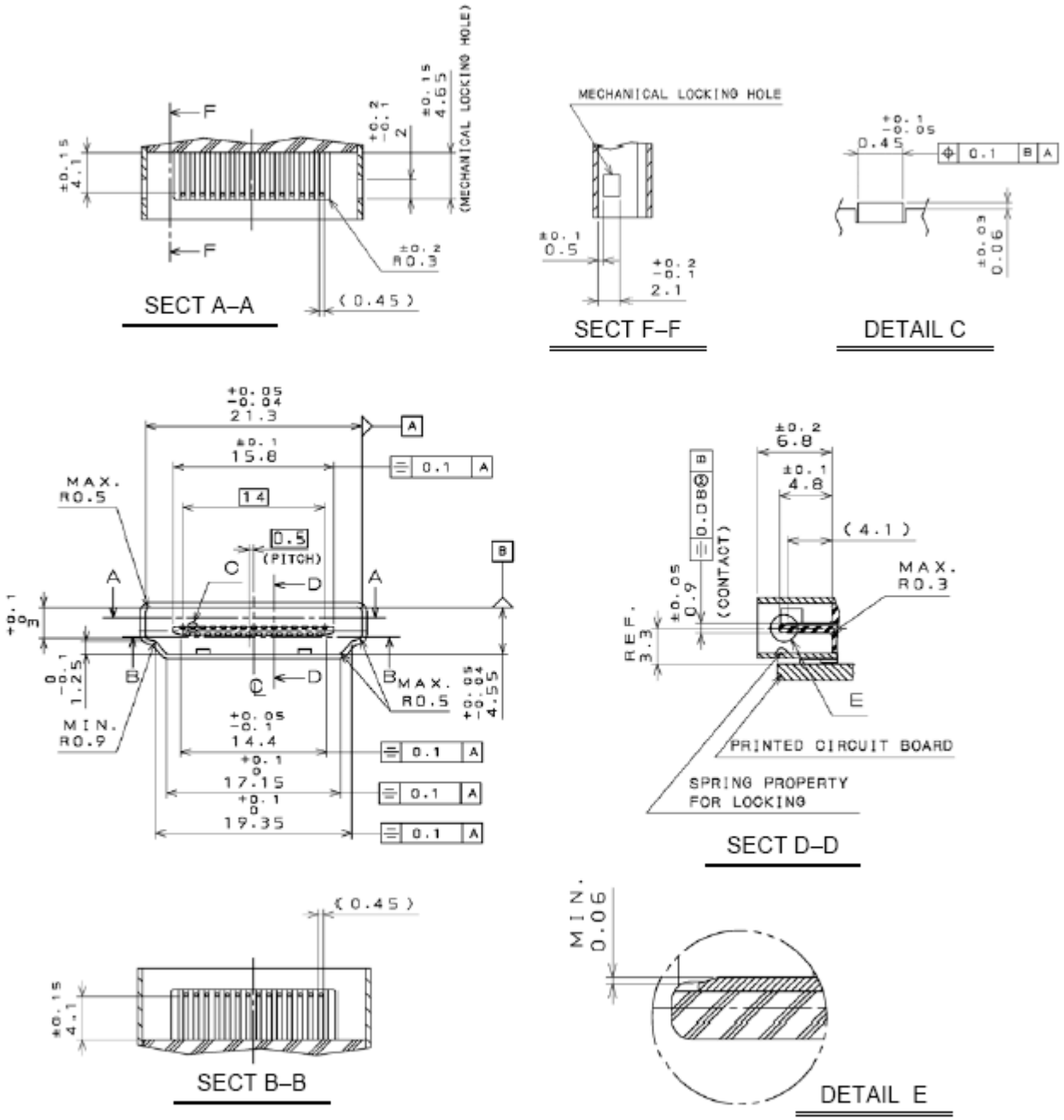
7.3.1 Mechanical – HDMI-A



- The shell shall have springs for locking. Additional springs may be used for EMI reduction.
- The spring property for locking shall be activated by the locking hole of the plug shell.

Figure 7-4: HDMI-A Connector

7.3.2 Mechanical – HDMI-B



- The shell shall have springs for locking. Additional springs may be used for EMI reduction.
- The spring property for locking shall be activated by the locking hole of the plug shell.

Figure 7-5: HDMI-B Connector

7.3.3 HDMI Connector Pin-outs

Table 7-3: HDMI-A & HDMI-B Connector Pin-outs

HDMI-A Connector		HDMI-B Connector	
Pin number	**Signal**	**Pin number**	**Signal**
1	TMDS data 2+	1	TMDS data 2+
2	TMDS data 2 shield	2	TMDS data 2 shield
3	TMDS data 2-	3	TMDS data 2-
4	TMDS data 1+	4	TMDS data 1+
5	TMDS data 1 shield	5	TMDS data 1 shield
6	TMDS data 1-	6	TMDS data 1-
7	TMDS data 0+	7	TMDS data 0+
8	TMDS data 0 shield	8	TMDS data 0 shield
9	TMDS data 0-	9	TMDS data 0-
10	TMDS clock+	10	TMDS clock+
11	TMDS clock shield	11	TMDS clock shield
12	TMDS clock-	12	TMDS clock-
13	CEC (Consumer electronic control)	13	TMDS data 5+
14	Reserved	14	TMDS data 5 shield
15	SCL (Serial clock line)	15	TMDS data 5-
16	SDA (Serial data line)	16	TMDS data 4+
17	DDC / CEC ground	17	TMDS data 4 shield
18	+5 volt power	18	TMDS data 4-
19	Hot plug detect	19	TMDS data 3+
		20	TMDS data 3 shield
		21	TMDS data 3-
		22	CEC (Consumer electronic control)
		23	Reserved
		24	Reserved
		25	SCL (Serial clock line)
		26	SDA (Serial data line)
		27	DDC / CEC ground
		28	+5 volt power
		29	Hot plug detect

7.3.4 Power Requirements

Check the HDMI specification for details of the voltage and current limits on the +5 volt line.

7.4 DisplayPort

Note: This information is provided for information only. User is advised to verify accuracy by checking the latest version of the DisplayPort Standard – in the event of conflict, the DisplayPort Standard must be considered correct.

7.4.1 Mechanical – External DisplayPort

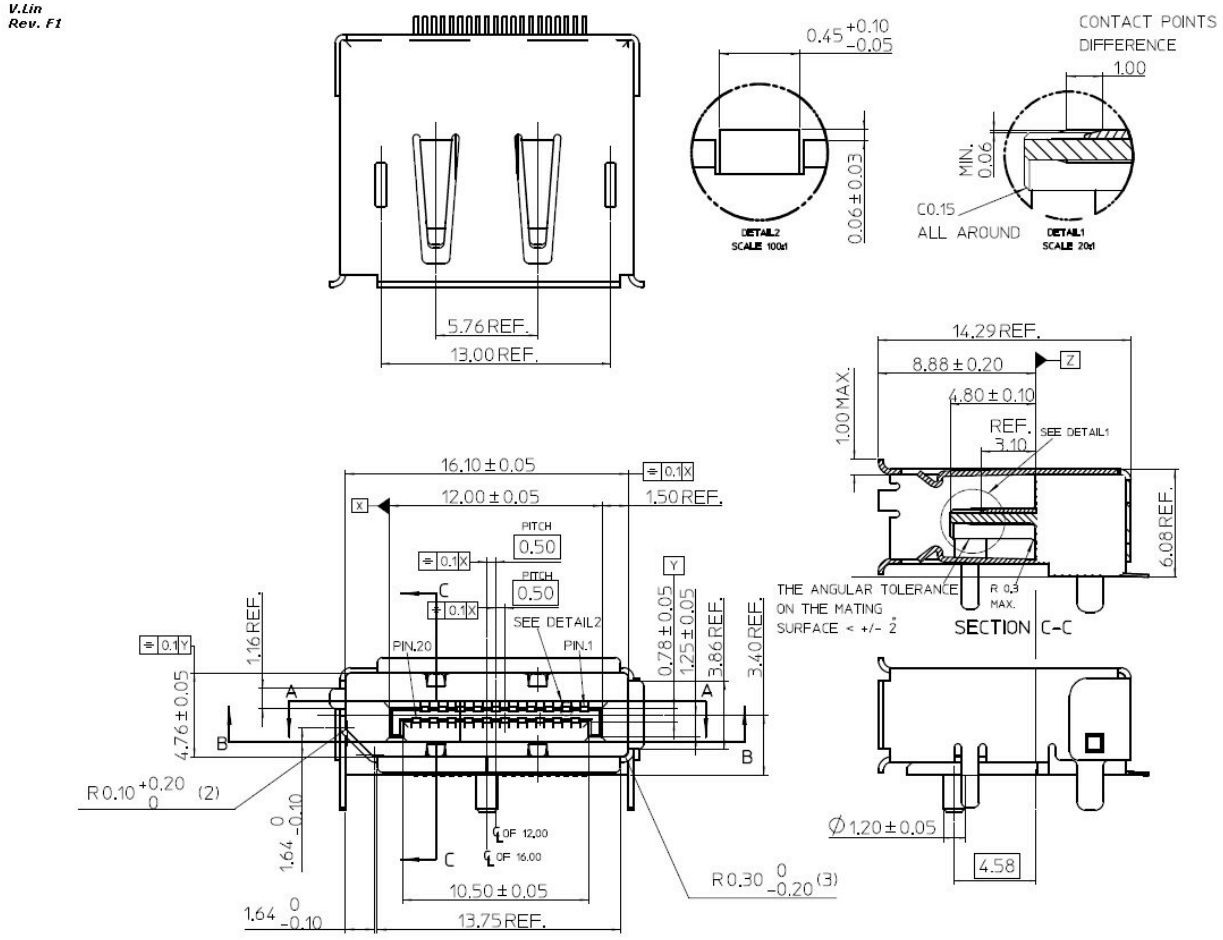


Figure 7-6: DisplayPort External Connector Receptacle

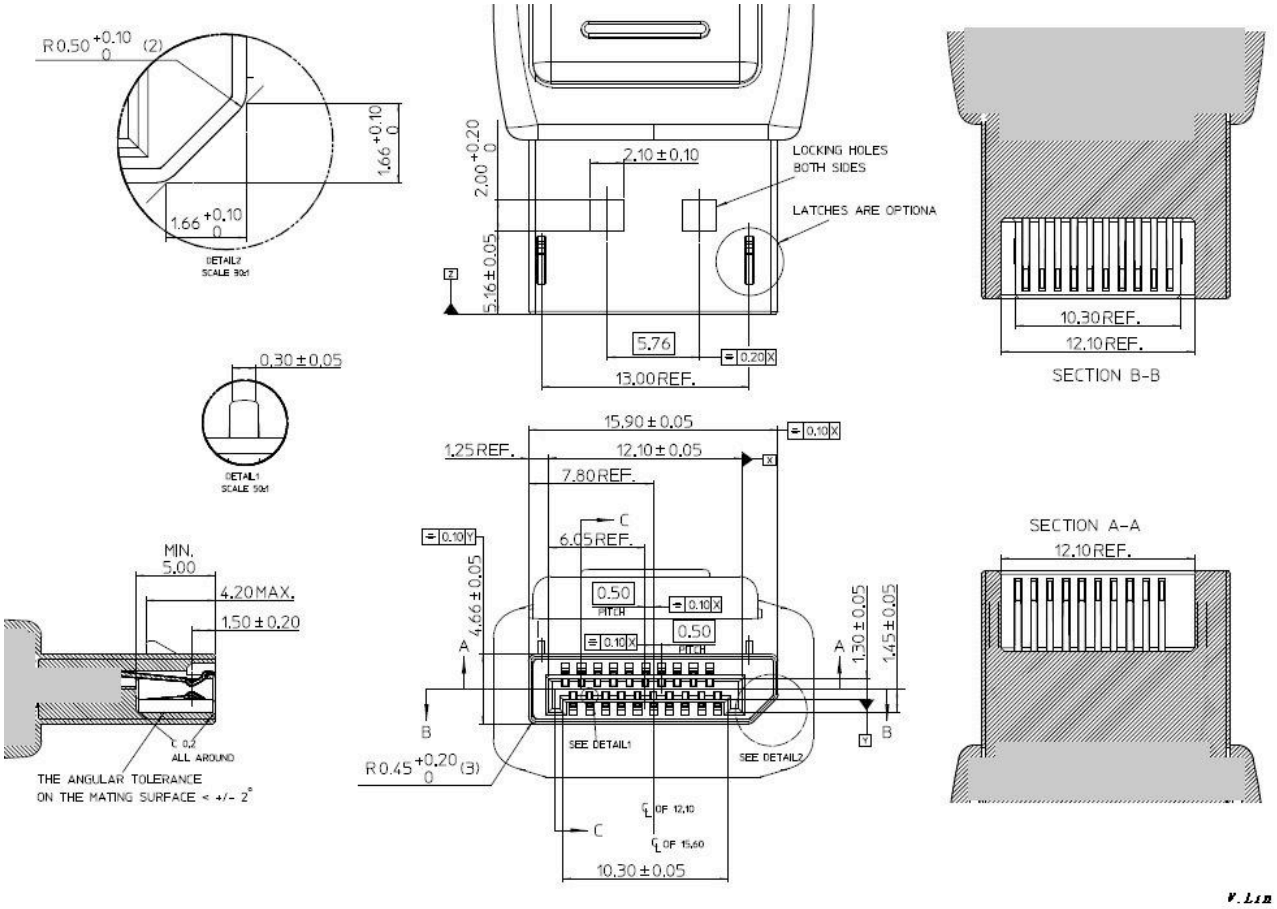


Figure 7-7: DisplayPort External Connector Plug

7.4.2 DisplayPort External Connector Pin-Out

Table 7-4: DisplayPort External Connector Pin-out

Pin Number	Signal	Pin Number	Signal
1	ML_Lane 0(p)	11	
2		12	ML_Lane 3 (n)
3	ML_Lane 0 (n)	13	
4	ML_Lane 1 (p)	14	
5		15	AUX CH (p)
6	ML_Lane 1 (n)	16	
7	ML_Lane 2 (p)	17	AUX CH (n)
8		18	Hot Plug Detect
9	ML_Lane 2 (n)	19	
10	ML_Lane 3 (p)	20	DP_PWR

7.4.3 Power Requirements

Check the DisplayPort standard for details of the voltage and current limits on the power pin.

8. DisplayPort and DDC/E-DDC

The DisplayPort interface standard provides support for E-DDC but does not implement this over an I^2C bus. Instead, DisplayPort uses its auxiliary (AUX) channel to carry E-DDC and E-EDID or DisplayID commands and data. This mapping of I^2C bus transactions to and from the DisplayPort AUX channel is transparent and requires no additional action by the I^2C host or slave device.

Figure 8-1, taken from the DisplayPort Standard, shows a block diagram of the AUX channel portion of a DisplayPort link between a desktop PC and a monitor.

In the desktop PC an I^2C bus associated with the GPU (Graphic Processing Unit) connects to the DisplayPort transmitter. The transmitter will act as an I^2C slave but also map the I^2C command and data structure on the AUX channel.

In the DisplayPort receiver the AUX channel will map the command and data structure back to I^2C format and act as a master for the local I^2C slave device.

In this example, the GPU (I^2C master) and EDID (I^2C slave) have no way of knowing that they are not communicating directly with each other, that for part of the transmission path the signal is being carried over the DisplayPort AUX channel.

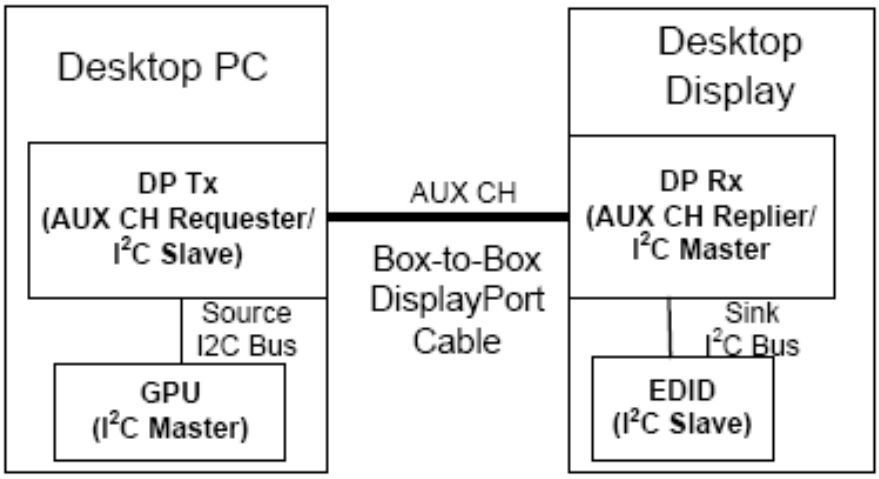


Figure 8-1: DisplayPort Mapping of I^2C to AUX Channel

See the DisplayPort Standard for further details.

9. Enhanced DDC System / Display Combinations

This section addresses issues that may arise in computer / display systems.

9.1 Interoperability

There are two scenarios that can occur where the display and host system support different versions of EDID standards. This potentially raises issues of compatibility and interoperability between the standards which are discussed in the following sections.

9.1.1 DDC Host System Connected to an E-DDC Display

The first scenario of potential concern is that of a DDC compliant host connected to a display that supports the E-DDC standard. This situation is addressed by the full backward compatibility of the E-DDC standard.

A unique situation can potentially occur where a DDC graphics sub-system uses a driver (software or firmware) to utilize the extended features of the proposed new standard. In this situation it is possible that a system reset can be initiated while the software driver is performing an extended EDID (or DisplayID) operation in which the segment pointer register has been set to point to a segment other than segment 0.

If the extended EDID (or DisplayID) operation has not been completed when the host resets, then the segment pointer register will not be reset and the graphics controller BIOS would then be unable to recognize the display. In order to address this issue, the E-DDC standard requires that the segment pointer register must be reset to 00h when a NO ACK or a STOP condition is received.

9.1.2 Enhanced DDC Host Connected to a DDC Display

The second scenario is one in which the graphics controller supports the Enhanced EDID (or DisplayID) standard, and the monitor is DDC compliant only.

In this case, the system issues the START condition and the DDC address byte for the Enhanced EDID command for the segment pointer register at 60h but the display will not respond to this address - in effect the display issues a NO ACK.

Since a NO ACK is a valid response, the host will continue by writing the segment pointer.

Note: Since the host cannot assume that there are any other segments than segment 0, the segment pointer register must be set for segment 0 in order to read EDID or DisplayID.

The display will once again not respond, in effect issuing a NO ACK. Also here, the NO ACK is a valid response and the host will continue with the read process.

The rest of the process is identical to a DDC EDID (or DisplayID) read operation and the display will respond with its EDID (or DisplayID).

10. E-DDC Compliance

Compliance with the VESA E-DDC Standard requires that all requirements of Sections 1.1 to 8 inclusive are met.

10.1 Older Designs

Older DDC displays and graphics subsystem designs will generally comply with the DDC standard versions 1, 2 or 3 only and not support the new features added in the E-DDC standard.

Designs based on the DDC1 protocol are not compliant with the E-DDC standard; DDC1 is not recommended for any new design and is no longer supported by VESA.

10.2 New Display Designs

It is strongly recommended that new DDC monitor designs comply with E-DDC Standard Version 1.2 (this standard) including the ability for the host to read EDID and DisplayID structures when the display is powered 'off' to enable plug and play operation.

Note: Displays are not required to implement the segment pointer if all data can be accessed in segment 0.

10.3 New Host Subsystem Designs

It is strongly recommended that new DDC host designs comply with E-DDC Standard Version 1.2 (this standard).

Note: Designs compliant with DDC Standard Version 3 or earlier may not be able to access the complete data in an E-DDC display.

10.4 I^2C Bus

It is recommended that the correct operation of I^2C in VGA, DVI, HDMI etc interfaces is verified using commercial serial bus test equipment from a reputable manufacturer.

10.5 E-DDC Unique Features

Sections 10.5.1 to 10.5.3 inclusive outline compliance procedures for the unique features of the E-DDC standard.

10.5.1 Segment Pointer

Correct operation of the segment pointer register at address 60h has several test stages; compliance requires that all test stages are successfully completed.

Table 10-1: Segment Pointer Tests

Test	Requirement
Value written to the segment pointer register	Ensure that the correct area of the EDID or DisplayID memory is accessed when different values are written to the segment pointer register.
Segment pointer register reset	Verify that the segment pointer register is reset = 00h at the end of each command (normal operation).
Segment pointer register reset	Verify that the segment pointer register is reset = 00h on receipt of a NO ACK or STOP condition. See section 2.2.5

Test	Requirement
Write to address 60h when segment pointer register does not exist	Verify that the first 256 bytes of the EDID or DisplayID memory space can be read following an attempt to write to a non-existent segment pointer register. See section 2.2.5

10.5.2 Power Pin

Table 10-2: Power Pin Tests

Test	Requirement
+5 volt available	Verify that +5 volt supply is available. See section 7.1.3 for requirements on VGA interface. See appropriate standard for requirements on other interfaces.
Over current protection	Verify that the over current protection on the +5 volt line operates as specified. See section 7.1.3 for requirements on VGA interface. See appropriate standard for requirements on other interfaces.

10.5.3 EDID / DisplayID Available with Display Powered Off

Table 10-3: EDID and/or DisplayID Read with no Display Power

Test	Requirement
Read EDID and / or DisplayID with display in power off state.	Verify that EDID and / or DisplayID can be read correctly.

Note: In the case of hybrid devices using fiber optic and / or wireless communication for part of an interface, it may not be possible to read EDID or DisplayID with the display powered off.

10.6 Co-existence of E-DDC, DDC/CI and HDCP

Care must be taken if the E-DDC link is being used for multiple purposes. For example, if may be used for recovery of EDID, for control of the display (see VESA DDC/CI and MCCS standards) and for key exchange in HDCP scheme.

HDCP has a number of maximum response times for communication and, if these are exceeded communication will be interrupted - see the HDCP System specification, version 1.2 or later.

Caution: All designers and users of the E-DDC channel must ensure that they are compliant with the appropriate standards and, in particular, that control of the bus is released whenever possible.

11. Appendix A: Answers to Commonly Asked Questions

Note: This appendix is for information only.

Table 11-1: Answers to Commonly Asked Questions about E-DDC and the VGA Interface

	Question	Answer
1	Why is +5 volts on pin 9 of the VGA connector mandatory for hosts and/or graphic cards?	Reference: Section 7.1.3 It allows for EDID or DisplayID to be available to the host even if the user has not switched on the display i.e. it enables display plug and play by making it independent of the host and display power on sequence. It has become common for system management software to interrogate peripheral devices for product type and serial number as a form of asset management. This is usually scheduled for nighttime but if the display is powered off then no data can be collected. Providing +5 volts allows the DDC circuit in the display to remain active even when the display itself is powered off.
2	Is +5 volts mandatory for portable computers?	Reference: Section 7.1.3.1 Portable computers that want to be able to claim compliance with VESA E-DDC standard version 2 (and later) must provide the +5 volt output.
3	Is +5V from the host required to be continuously active?	Reference: Section 7.1.3.1 No, +5V must be provided whenever the host video port is active, or when the host is attempting to read the monitor's EDID data. In particular, hosts running on battery power may disable the +5V output when the host video port is not active, to conserve battery power.
4	Will +5 volt supply continue to be required?	As noted in section 7.1.3 there is currently a requirement for the host device to supply 5 volts ± 5% to the display to ensure that the EDID data can be read even if the display is switched off.
5	Is clock stretching required?	Reference Section 2.2.1 Yes, compliance with VESA E-DDC standard requires that the requirements of the I^2C specification are fully met.

	Question	Answer
6	What are the intended uses for the +5V output?	Ref.: Sections 7.1.3 & see note below. +5V is needed as a power source for the DDC and EDID circuits of a display when the host is attempting to read the monitor's EDID data and the display's own local power supply is not turned on. This capability is especially important when a host is initially booting up or when a mobile host user enables the external video port, so that the host can properly detect the type of display attached. This is the main use of +5V defined in the Enhanced DDC Standard. (The EDID and DDC circuits in a display should always be powered from the display's own local power supply whenever it is available.) The E-DDC Standard does not directly define or constrain other possible uses for the +5V output, provided that the specified load limits are not exceeded. For example, when the display is powered on, +5V may be used as a logic signal to control display power states: i.e., Signaling to the display whether or not the host video port is active, so that the display can decide when to go into a reduced power mode. This is the reason why the +5V must be provided continuously whenever the host video port is active. Since the host might be a portable device running on battery power, the total load on the +5V from the host must be limited to 1 mA maximum when the display has local power.

Notes:

1) Check the VESA DisplayPort Standard for similar guidance.

2) Check with the organizations responsible for the DVI (see www.ddwg.org) and HDMI (see www.hdmi.org) specifications for similar guidance.

12. Appendix B: Main Contribution History

Table 12-1: Main Contributors to E-DDC Version 1.0

Name	Company
David Johnson	Intel
Jack Hosek	NEC
Anders Frisk	Nokia
Nathan John	Microchip Technology
Rick Stoneking	Microchip Technology
John Matsumoto	Toshiba

Table 12-2: Main Contributors to E-DDC Version 1.1

Name	Company	
Syed Athar Hussain	ATI Technologies Inc.	
Chi Tai Hong	Chrontel, Inc.	
Joe Goodart	Dell	
Graham Loveridge	Genesis Microchip	
Jim Webb	Genesis Microchip	
Bob Myers	Hewlett-Packard	
Ian Miller	Samsung	Workgroup leader
Joe Lamm	Tech Source	
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